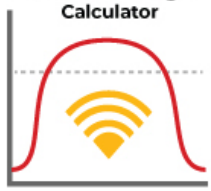
SIERRA CIRCUITS

CONTROLLED IMPEDANCE

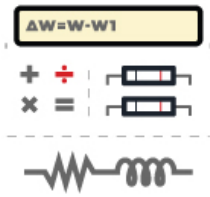
DESIGN GUIDE

The Designer's Toolkit

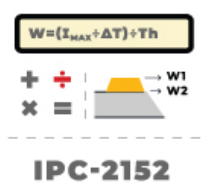
Bandwidth, Rise Time and Critical Length Calculator



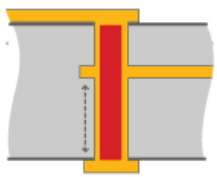
Impedance Calculator



Trace Width, Current and Temp Rise Calculator

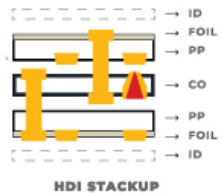


Maximum Via Stub Length Calculator



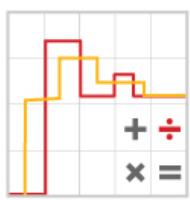
PCB Material Selector

PCB Stackup Designer

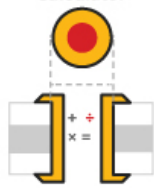


Signal Layer Estimator

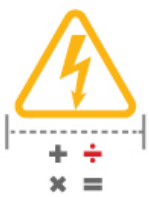
Transmission Line Reflection Calculator



Via Current Capacity and Temperature Rise Calculator

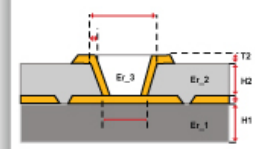


PCB Conductor Spacing and Voltage Calculator



RLC Resonant Frequency & Impedance Calculator

Via Impedance Calculator



BOM Checker

TRY TOOLS

Better DFM

Greetings:

Sierra Circuits has proudly served more than 20,000 PCB designers and engineers since 1986. Our customers rely on us for the design, manufacturing and assembly of their printed circuit boards. As PCBs grow smaller and trace & space becomes tighter, reliable microelectronics have a larger emphasis in our field.

We deliver high-quality HDI PCBs, and handle all aspects of PCB assembly, from PCB layout and design to assembly and manufacturing. We aim to simplify your PCB fabrication and assembly process. Our services include turnkey, consigned and partially consigned assembly. and microelectronics. We provide customers with quality, reliability, and a single point of support from our Silicon Valley facilities.

If there is anything we can do to assist you with your next project, let us know.

We look forward to working with you!

Ken Bahl

President
Sierra Circuits

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1.Overview

1.1 What is controlled impedance?

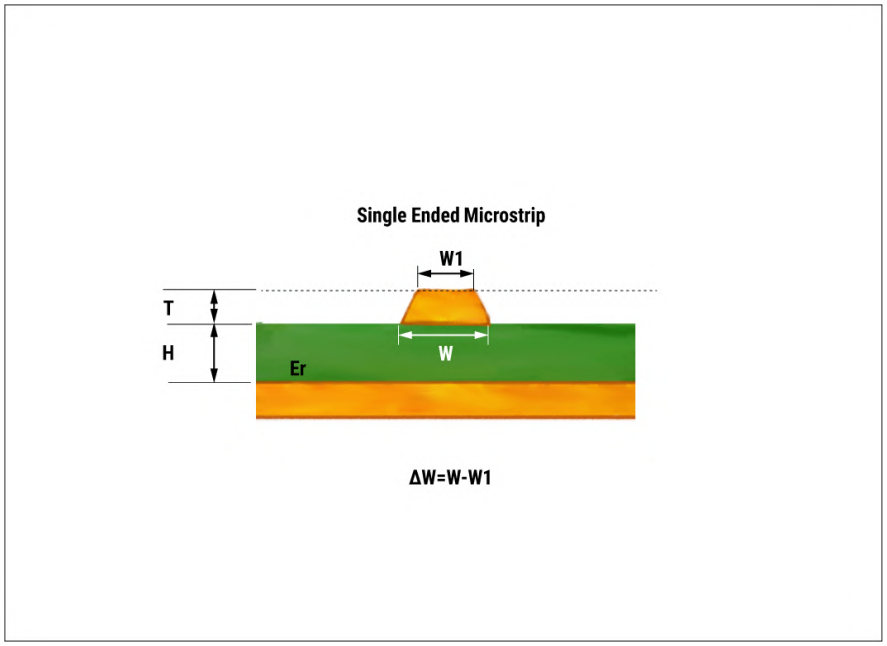
Controlled impedance is the characteristic impedance of a transmission line formed by a PCB trace and its associated reference planes. It is relevant when high-frequency signals propagate on the PCB transmission lines. A uniform controlled impedance is important for achieving good signal integrity, which is the propagation of signals without significant distortion.

The controlled impedance of PCB traces is determined by their physical dimensions and the property of the dielectric material used in the board. Controlled impedance is measured in ohms (Ω). Controlled impedance is important for telecommunications, video signal processing, high-speed digital processing, real-time graphic processing, and process control. It is also crucial for high-speed frequencies (above 100MHz).

The most common examples of the PCB transmission lines which require controlled impedance are **single-ended microstrip, single-ended stripline, microstrip differential pair, stripline differential pair, embedded microstrip, and coplanar (single-ended and differential).** When you look at the stack-up of a multilayer PCB, notice that controlled impedance traces are sandwiched between power and ground planes. The controlled impedance traces require solid ground planes/power planes, and the impedance depends on the distance of the trace from these planes.

1.1.1 Single-ended microstrip

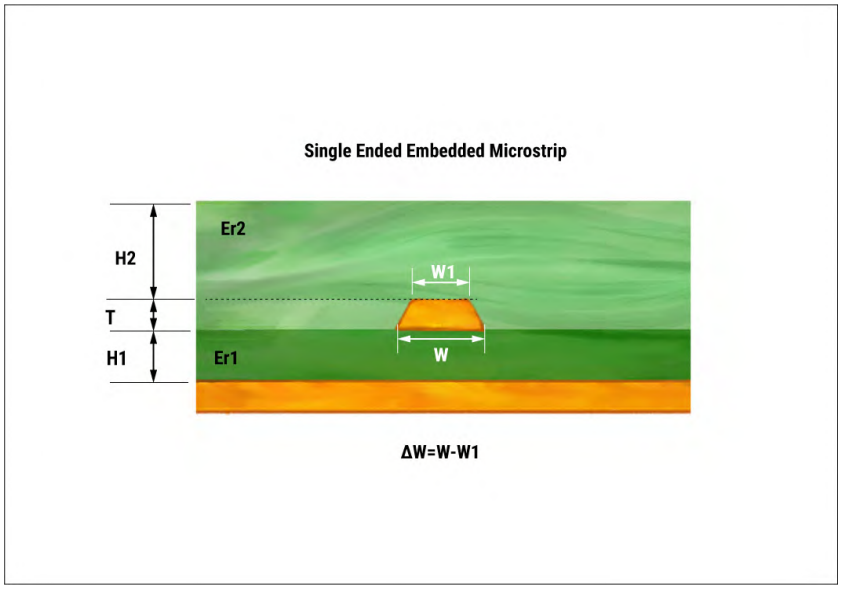
It is a transmission line on the outer layer of a PCB composed of a single uniform conductor. The return path for signals traveling on this line is usually provided by a conducting plane separated from the transmission line by a dielectric of a certain height.



H = height of the dielectric between the trace & plane, specified in mils
W = width of the copper trace, specified in mils
T = thickness of the copper trace, specified in mils
Er = dielectric constant of the dielectric between the trace & plane
ΔW = difference between the width at the top of the trace and the bottom of the trace

1.1.2 Single-ended embedded microstrip

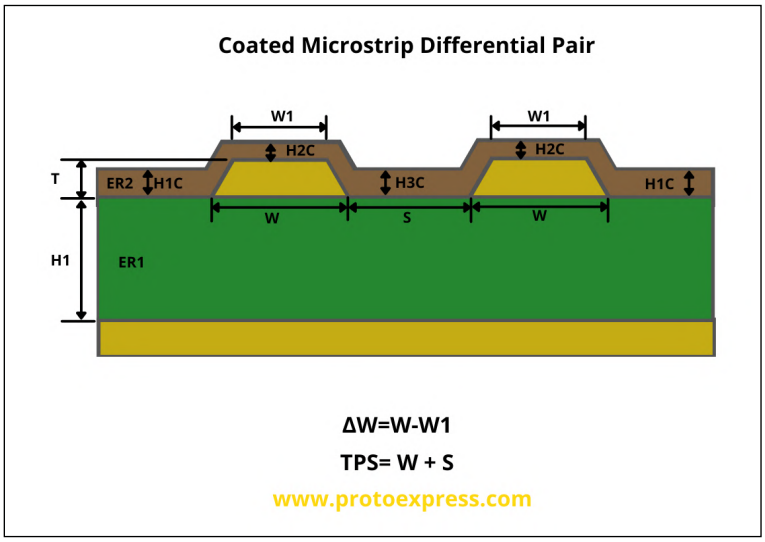
This structure is similar to a regular microstrip, except that there is another dielectric layer above the transmission line.



H1 = height of the first dielectric, specified in mils
H2 = height of the second dielectric, specified in mils
W = width of the copper trace, specified in mils
T = thickness of the copper trace, specified in mils
Er1 = dielectric constant of the first dielectric
Er2 = dielectric constant of the second dielectric
ΔW = difference between the width at the top of the trace and the bottom of the trace

1.1.3 Coated microstrip differential pair

This technique is used for routing differential pairs and has the same arrangement as regular microstrip routing. It is more complex due to the additional trace spacing required for the differential pair. It consists of a differential configuration with two controlled impedance traces on the surface, separated by a uniform distance and backed by a plane on the other side of the laminate.

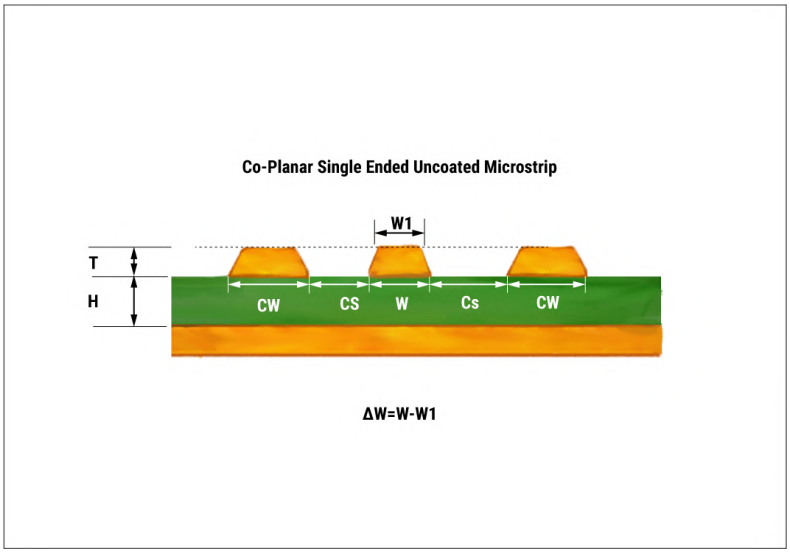


H1 = height of the dielectric between the trace & plane, specified in mils
W = width of the copper trace, specified in mils
T = thickness of the copper trace, specified in mils
Er1 = dielectric constant of the dielectric between the trace & plane
Er2 = coating dielectric constant
S = the separation between the two traces of the differential pair
TPS = trace width plus spacing between two conductors
ΔW = difference between the width at the top of the trace and the bottom of the trace

1.1.4 Coplanar single-ended uncoated microstrip

In a coplanar microstrip, the signal trace is routed in parallel to two ground planes. These ground planes provide natural shielding for the signal against interference from other traces on a board. It has a single controlled impedance trace with planes on either side (or very wide ground traces), a continuous plane on one side, and laminate only on the other side. There are two types of co-planar models; one with a ground plane below the trace and one without a ground plane.

The coplanar structure has the signal trace and the return path conductor on the same layer of the PCB. The signal trace is at the center and is surrounded by two adjacent outer ground planes; it is called 'coplanar' because these three flat structures are on the same plane.

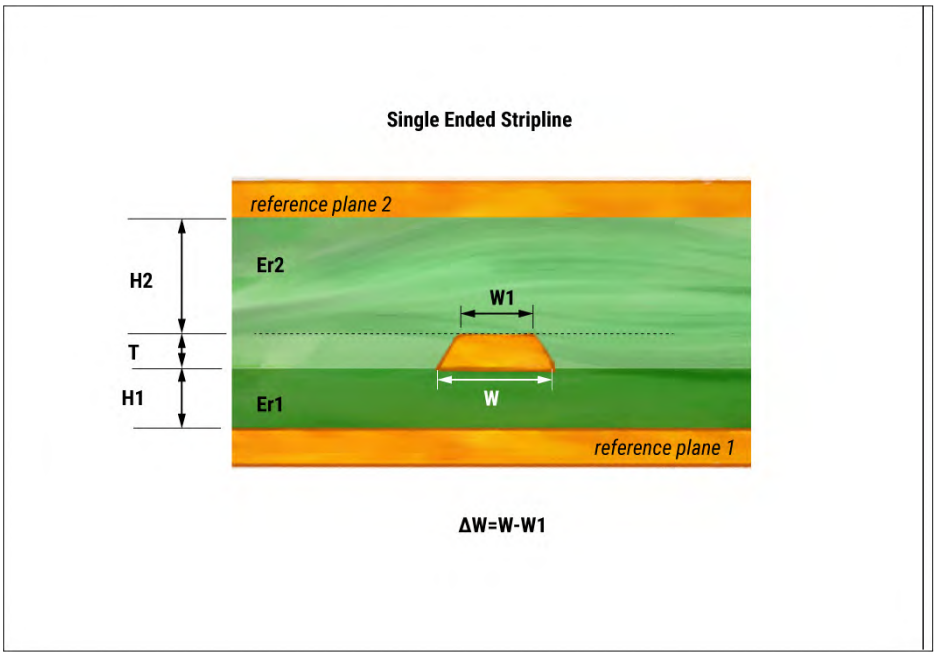


H = height of the dielectric between the trace & plane, specified in mils
W = width of the copper trace, specified in mils
T = thickness of the copper trace, specified in mils
Er = dielectric constant of the dielectric between the trace & plane
CS = coplanar spacing between ground planes and trace
CW = coplanar width
ΔW = difference between the width at the top of the trace and the bottom of the trace

1.1.5 Single-ended stripline

A single-ended stripline structure is composed of a uniform conductor on an inner layer of a PCB separated on each side by a dielectric layer followed by copper planes.

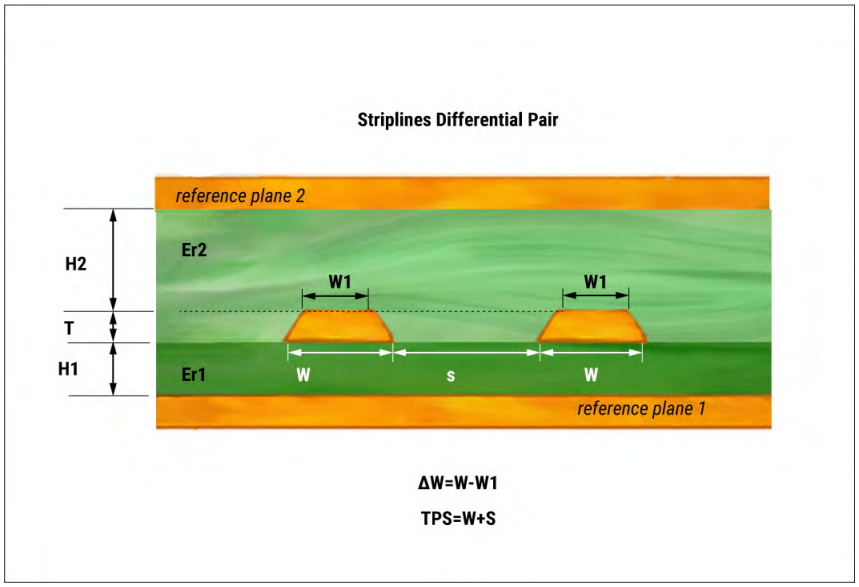
This arrangement implements the signal trace between two ground planes in a multi-layer PCB (signal trace between a power plane and a ground plane is rare). The return current path for a high-frequency signal trace is located above and below the signal trace on the planes. So, the high-frequency signal remains inside the PCB, resulting in fewer emissions and shielding from other spurious signals.



H1 = height of the dielectric between the trace & reference plane 1, specified in mils
H2 = height of the dielectric between the trace & reference plane 2, specified in mils
W = width of the copper trace, specified in mils
T = thickness of the copper trace, specified in mils
Er1 = dielectric constant of the dielectric between the trace & reference plane 1
Er2 = dielectric constant of the dielectric between the trace & reference plane 2
ΔW = difference between the width at the top of the trace and the bottom of the trace

1.1.6 Striplines differential pairs

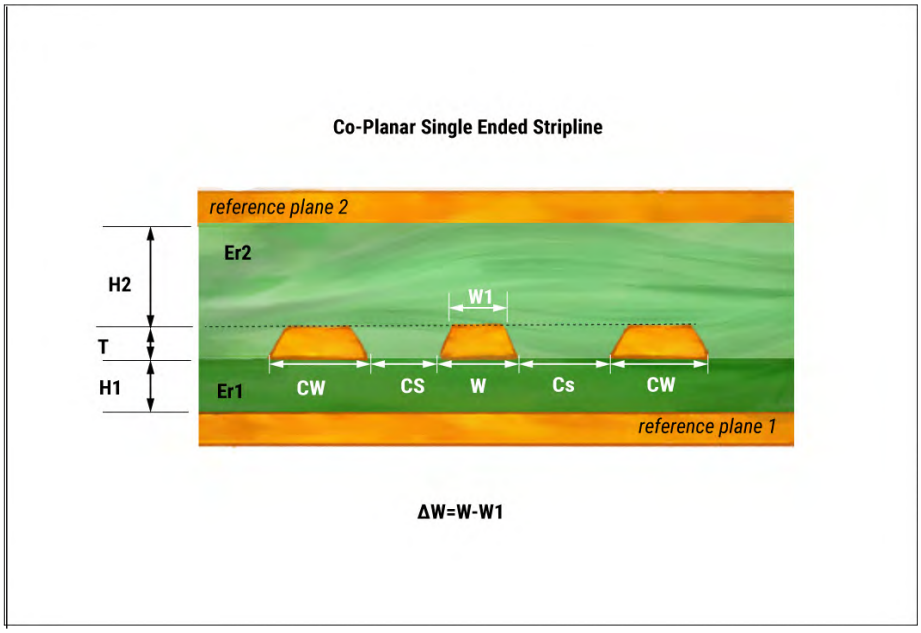
It is similar to the single-ended stripline described above, except that we now have a pair of conductors separated by a uniform distance between them. It is a differential configuration with two controlled impedance traces sandwiched between two planes.



H1 = height of the dielectric between the trace & reference plane 1, specified in mils
H2 = height of the dielectric between the trace & reference plane 2, specified in mils
W = width of the copper traces, specified in mils
T = thickness of the copper traces, specified in mils
Er1 = dielectric constant of the dielectric between the trace & reference plane 1
Er2 = dielectric constant of the dielectric between the trace & reference plane 2
S = the separation between the two traces of the differential pair
ΔW = difference between the width at the top of the trace and the bottom of the trace
TPS = trace width plus spacing between two conductors

1.1.7 Coplanar single-ended stripline

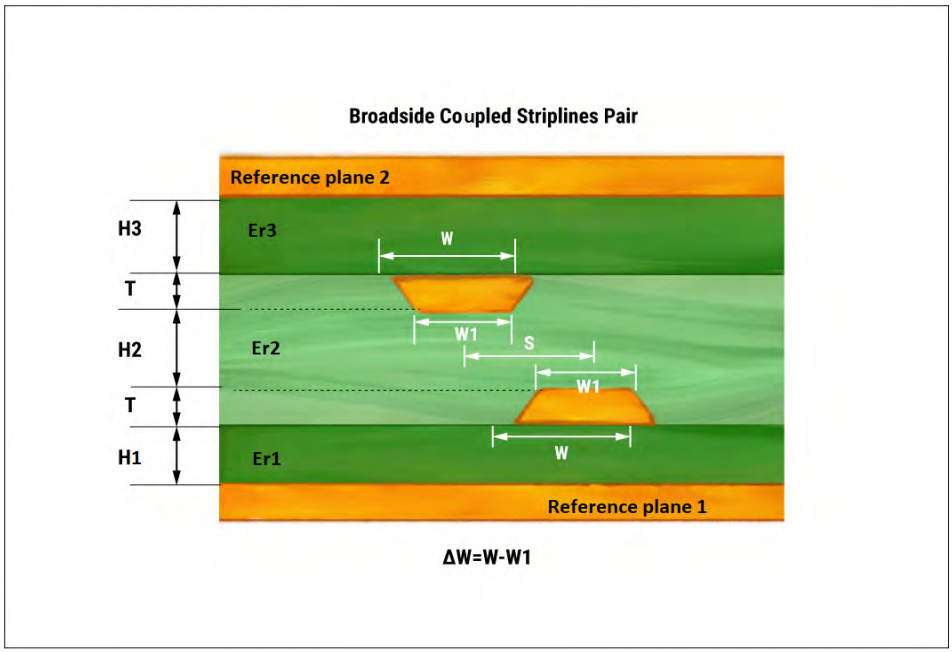
This structure consists of planes on both sides of the laminate and a plane on the same layer as the controlled impedance trace.



H1 = height of the dielectric between the trace & reference plane 1, specified in mils
H2 = height of the dielectric between the trace & reference plane 2, specified in mils
W = width of the copper trace, specified in mils
T = thickness of the copper trace, specified in mils
Er1 = dielectric constant of the dielectric between the trace & reference plane 1
Er2 = dielectric constant of the dielectric between the trace & reference plane 2
CS = coplanar spacing between ground planes and trace
CW = coplanar width
ΔW = difference between the width at the top of the trace and the bottom of the trace

1.1.8 Broadside coupled striplines pair

This technique is used for routing internal layer differential pairs. This differential configuration has two traces that are separated by a laminate and sandwiched between two planes. Although the diagram shows the offset traces, the manufacturing objective is to have the traces with no offset, i.e., one should be directly above the other. Typically, this configuration is difficult to fabricate.



H1 = height of the dielectric between the trace & reference plane 1, specified in mils
H2 = height of the dielectric between two traces, specified in mils
H3 = height of the dielectric between the trace & reference plane 2, specified in mils
W = width of the copper traces, specified in mils
T = thickness of the copper traces, specified in mils
Er1 = dielectric constant of the dielectric between the trace & reference plane 1
Er2 = dielectric constant of the dielectric between the traces
Er3 = dielectric constant of the dielectric between the trace & reference plane 2
ΔW = difference between the width at the top of the trace and the bottom of the trace

1.2 When and why do you need controlled impedance?

Typically, you will need controlled impedance for PCBs used in high-speed digital applications, such as RF communication, telecommunications, computing using signal frequencies above 100MHz, and high-speed signal processing and high-quality video such as DDR, HDMI, Gigabit, and Ethernet, etc.

At high-frequency, the signal traces on a PCB act like transmission lines, which have impedance at each point on the signal trace trajectory. If this impedance varies from one point to the next, there will be a signal reflection whose magnitude will depend on the difference between the two impedances. The larger difference is, the greater the reflection will be. This reflection will travel in the opposite direction of the signal, which means that the reflected signal will superimpose on the main signal. As a result, the original signal will be distorted; the signal intended to be sent from the transmitter side would have changed once it got to the receiver side. The distortion may be so much that the signal may not be able to perform the desired function. Therefore, to have undistorted signal travel, the PCB signal traces have a uniform controlled impedance to minimize signal distortions caused by reflections. This is the first step to improve the integrity of the signals on the PCB traces.

A uniform transmission line on a PCB has a definite trace width and height and is at a uniform distance from the return path conductor - which is usually a plane at a certain distance from the signal trace.

Standard tolerance for controlled impedance is +/- 10% ohms. If you need a tighter tolerance, call Sierra Circuits at (800) 763-7503 as we also offer +/-5% ohms.

1.3 What affects impedance?

In summary, as stated in some of the PCB transmission line models in section 1.1, the impedance of PCB signal traces is affected by:

- The height of the dielectric layer between the signal trace and the reference planes
- The width and the thickness of the signal trace
- The dielectric constant of a dielectric material
- The spacing between differential pairs traces

PCB dielectric materials used in board constructions are categorized into two types: copper clad cores and prepregs. The various types of cores and the prepregs usually have different dielectric constants, as specified in the detailed data available from the laminate manufacturer.

Keep in mind that the impedance of traces is defined by more than the size of the trace. When you define a trace as a controlled impedance trace, the impedance matters more than the size of the feature for PCB manufacturers. So they might change certain specifications you gave in your Gerber files such as the trace width, the trace height, and the dielectric thickness. But they will make sure that the final impedance is within the tolerance.

1.4 Trace impedance (Characteristics impedance)

Special care should be taken to distinguish between single-ended and differential trace impedance. High-speed single-ended signals such as the parallel RGB LCD or camera interface need to be routed with the specified single-ended impedance. It is the impedance between the trace and the reference ground. On the other hand, high-speed differential pair signals such as SATA, PCIe, HDMI, USB, etc., require routing with differential impedance. It is the impedance between the two signal traces of a pair.

When selecting trace geometry, priority should be given to matching the differential impedance over the single-ended impedance. The differential impedance is always smaller than twice the single-ended impedance.

$$Z_{Differential} < 2.\ Z_{Single\text{-}ended}$$

Try to keep the calculated impedance value as close as possible to the exact impedance value. This allows greater flexibility during PCB manufacture.

1.5 Specifying a controlled dielectric board instead of controlled impedance

You can get controlled impedance in two ways: first is to specify the dielectric thicknesses that you are looking for in your fabrication drawing and not specify any of the controlled impedance parameters at all. The second method, which we think is the better way, is to specify the layers in which you'd like your impedance lines on and the target ohms. Standard tolerance is +/- 10% ohms. If tighter tolerance is needed, we can deliver +/- 5% ohms. Tighter tolerance would require a different game plan ahead of time. Samples of fabrication notes can be found in section 3.6. Manufacturers can now model controlled impedance more accurately using new tools and detailed data about PCB materials.

- **Controlled dielectric thickness:** The designer provides the controlled di electric stack-up to the manufacturer. Since impedance traces are not spec ified here, the manufacturing focus is completely upon building a board with in +/- 10% tolerance of the specified dielectric thickness from layer to layer.

- **Impedance control:** Here, the impedance is controlled through the dielectric thickness, the trace width, and space. The manufacturer performs a test to ensure that the desired impedance can be achieved using TDR cou pons. Some adjustments are made depending upon results from the first articles to meet the designer's needs, and the boards are manufactured within the specified tolerance.

2

2.Controlled impedance for manufacturing

2.1 Defining cores and prepregs

A multilayer board manufacturing requires two forms of PCB materials: cores and prepregs. Cores are copper-clad laminates. Their dielectric thickness does not vary after lamination because they are fully-cured materials (copper is on the outside).

Prepregs are semi-cured materials, and they are used as a bonding material between two core laminates. After lamination, the final thickness of a prepreg material depends on the percentage of the copper in the adjoining conducting layers, the height of the copper in these layers, and the type of prepreg used. All semi-cured prepregs are turned into fully-cured dielectric after the lamination process.

It is crucial that during the lamination process, a high degree of process control and integrity is maintained so that post-lamination thicknesses are reasonably predictable and the mechanical integrity of copper conductors is maintained. All of Sierra Circuits' lamination cycles have computer-controlled profiles to achieve consistency.

Here are some examples of PCB stack-ups:

6-layer stack-up:

6 Lay	Drills & µVias	Foil, Core or Prepreg Details	CU Oz / Th. Mils	Dk (10Ghz)	Plating Mils	6 L CI-1	Cu %	Final Thickness
		Solder mask	0.500	4.20				0.500
6L-1		CU Foil	0.25		1.1	S	100%	1.450
		4 Mil Prepreg	4.000	3.86				3.496
6L-2		Copper	1		0	P	64%	1.400
		5 Mil Core 1/1	5.000	3.84				5.000
6L-3		Copper	1		0	S	24%	1.400
		36 Mil Prepreg	36	4.16				33.872
6L-4		Copper	1		0	S	24%	1.400
		5 Mil Core 1/1	5.000	3.84				5.000
6L-5		Copper	1		0	P	64%	1.400
		4 Mil Prepreg	4.000	3.86				3.496
6L-6		CU Foil	0.25		1.1	S	100%	1.450
		Solder mask	0.500	4.20				0.500
		FINISHED PCB THICKNESS						60.364
		PCB thickness after Lamination						*57.164*
		# of Laminations: 1						

Impedance Models Examples

Signal layer	Ref_1 layer	Ht to Ref_1	Ref_2 layer	Ht to Ref_2	40 Ω SE	45 Ω SE	50 Ω SE	55 Ω SE	60 Ω SE	75 Ω Diff.		80 Ω Diff.		90 Ω Diff.		100 Ω Diff.		120 Ω Diff.	
					T	T	T	T	T	T	S	T	S	T	S	T	S	T	S
6L-L1	6L-L2	3.50	--	--	8.60	6.90	5.60	4.50	3.60			5.75	4.25	4.80	5.20	4.00	6.00	3.00	11.00
6L-L6	6L-L5	3.50	--	--						6.70	4.30	6.10	4.90	5.10	5.90	4.20	6.80		
All Impedances Applicable for 6L-L1 and 6L-L6										7.10	4.90	6.50	5.50	5.40	6.60	4.40	7.60		
										7.70	6.30	7.00	7.00	5.80	8.20	4.70	9.30		
6L-L3	6L-L2	5.00	6L-L5	41.66	10.70	8.60	6.80	5.50	4.40			5.80	4.20	4.80	5.20	3.90	6.10	3.00	9.70
6L-L4	6L-L5	5.00	6L-L2	41.66						6.80	4.20	6.20	4.80	5.20	5.80	4.20	6.80		
All Impedances Applicable for 6L-L3 and 6L-L4										7.30	4.70	6.70	5.30	5.50	6.50	4.50	7.50		
										8.20	5.80	7.40	6.60	6.10	7.90	4.90	9.10		

2

8-layer stack-up:

8 Lay	Drills & µVias	Foil, Core or Prepreg Details	CU Oz / Th. Mils	Dk (10Ghz)	Plating Mils	8 L CI-1	Cu %	Final Thickness
		Solder mask	0.500	4.20				0.500
8L-1		CU Foil	0.25		1.1	S	100%	1.450
		4 Mil Prepreg	4.000	3.86				3.496
8L-2		Copper	1		0	P	64%	1.400
		5 Mil Core 1/1	5.000	3.84				5.000
8L-3		Copper	1		0	S	24%	1.400
		8.8 Mil Prepreg	8.800	3.68				7.232
8L-4		Copper	1		0	P	64%	1.400
		18 Mil Core 1/1	18.000	4.15				18.000
8L-5		Copper	1		0	P	64%	1.400
		8.8 Mil Prepreg	8.800	3.68				7.232
8L-6		Copper	1		0	S	24%	1.400
		5 Mil Core 1/1	5.000	3.84				5.000
8L-7		Copper	1		0	P	64%	1.400
		4 Mil Prepreg	4.000	3.86				3.496
8L-8		CU Foil	0.25		1.1	S	100%	1.450
		Solder mask	0.500	4.20				0.500
		FINISHED PCB THICKNESS						61.756
		PCB thickness after Lamination						*58.556*
		# of Laminations: 1						

Impedance Models Examples

Signal layer	Ref_1 layer	Ht to Ref_1	Ref_2 layer	Ht to Ref_2	40 Ω SE	45 Ω SE	50 Ω SE	55 Ω SE	60 Ω SE	75 Ω Diff.		80 Ω Diff.		90 Ω Diff.		100 Ω Diff.		120 Ω Diff.	
					T	T	T	T	T	T	S	T	S	T	S	T	S	T	S
8L-L1	8L-L2	3.50	--	--	8.60	6.90	5.60	4.50	3.60			5.75	4.25	4.80	5.20	4.00	6.00	3.00	11.00
8L-L8	8L-L7	3.50	--	--						6.70	4.30	6.10	4.90	5.10	5.90	4.20	6.80		
All Impedances Applicable for 8L-L1 and 8L-L8										7.10	4.90	6.50	5.50	5.40	6.60	4.40	7.60		
										7.70	6.30	7.00	7.00	5.80	8.20	4.70	9.30		
8L-L3	8L-L2	5.00	8L-L4	7.23	7.60	6.20	5.00	4.00	3.20			5.50	4.50	4.50	5.50	3.70	6.30	3.00	14.70
8L-L6	8L-L7	5.00	8L-L5	7.23						6.50	4.50	5.90	5.10	4.80	6.20	3.90	7.10		
All Impedances Applicable for 8L-L3 and 8L-L6										6.80	5.20	6.20	5.80	5.10	6.90	4.10	7.90		
										7.40	6.60	6.70	7.30	5.50	8.50	4.40	9.60		

10-layer stack-up:

10 Laye	Drills & µVias	Foil, Core or Prepreg Details	CU Oz / Th. Mils	Dk (10Ghz)	Plating Mils	8 L CI-1	Cu %	Final Thickness
		Solder mask	0.500	4.20				0.500
10L-1		CU Foil	0.25		1.1	S	100%	1.450
		4 Mil Prepreg	4.000	3.86				3.496
10L-2		Copper	1		0	P	64%	1.400
		5 Mil Core 1/1	5.000	3.84				5.000
10L-3		Copper	1		0	S	24%	1.400
		8.8 Mil Prepreg	8.800	3.68				7.232
10L-4		Copper	1		0	P	64%	1.400
		4 Mil Core 1/1	4.000	3.84				4.000
10L-5		Copper	1		0	P	64%	1.400
		8.8 Mil Prepreg	8.800	3.68				7.792
10L-6		Copper	1		0	P	64%	1.400
		4 Mil Core 1/1	4.000	3.84				4.000
10L-7		Copper	1		0	P	64%	1.400
		8.8 Mil Prepreg	8.800	3.68				7.232
10L-8		Copper	1		0	S	24%	1.400
		5 Mil Core 1/1	5.000	3.84				5.000
10L-9		Copper	1		0	P	64%	1.400
		4 Mil Prepreg	4.000	3.86				3.496
10L-10		CU Foil	0.25		1.1	S	100%	1.450
		Solder mask	0.500	4.20				0.500
		FINISHED PCB THICKNESS						62.348
		PCB thickness after Lamination						*59.148*
		# OF LAMINATIONS: 1						

Impedance Models Examples

Signal layer	Ref_1 layer	Ht to Ref_1	Ref_2 layer	Ht to Ref_2	40 Ω SE	45 Ω SE	50 Ω SE	55 Ω SE	60 Ω SE	75 Ω Diff.		80 Ω Diff.		90 Ω Diff.		100 Ω Diff.		120 Ω Diff.	
					T	T	T	T	T	T	S	T	S	T	S	T	S	T	S
10L-L1	10L-L2	3.50	--	--	8.60	6.90	5.60	4.50	3.60			5.75	4.25	4.80	5.20	4.00	6.00	3.00	11.00
10L-L10	10L-L9	3.50	--	--						6.70	4.30	6.10	4.90	5.10	5.90	4.20	6.80		
All Impedances Applicable for 10L-L1 and 10L-L10										7.10	4.90	6.50	5.50	5.40	6.60	4.40	7.60		
										7.70	6.30	7.00	7.00	5.80	8.20	4.70	9.30		
10L-L3	10L-L2	5.00	10L-L4	7.23	7.60	6.20	5.00	4.00	3.20			5.50	4.50	4.50	5.50	3.70	6.30	3.00	14.70
10L-L8	10L-L9	5.00	10L-L7	7.23						6.50	4.50	5.90	5.10	4.80	6.20	3.90	7.10		
All Impedances Applicable for 10L-L3 and 10L-L8										6.80	5.20	6.20	5.80	5.10	6.90	4.10	7.90		
										7.40	6.60	6.70	7.30	5.50	8.50	4.40	9.60		

An important component of the PCB material is the resin content. The percentage of the resin content greatly impacts the final thickness and the dielectric constant: the higher the thickness, the lower the dielectric constant of the PCB material. For the same type of PCB material, different thickness cores (PCB laminates) and different prepregs have different resin contents, therefore different dielectric constants. When PCB manufacturers model the impedance traces, they take care of such fine variations in dielectric constants due to resin content.

The thickness and the dielectric constant of generic prepreg glass styles for Isola 370HR material are given in the chart below.

Prepreg Styles	Resin Content	Nominal Thickness (100% copper)	Dk at 5-10GHz
106	76%	2.3 mils	3.54
1086	63%	3.1 mils	3.78
1080	66%	3.0 mils	3.72
1080	68%	3.2 mils	3.68
1080	71%	3.6 mils	3.63
2113	59%	4.0 mils	3.86
2116	56%	4.8 mils	3.92

2.2 The PCB stack-up design

The stack-up design is very crucial for the design of a controlled impedance PCB. The designer needs to create a stack-up for the board and then calculate the trace values for differential pairs and single-ended nets. Designers can perform these tasks by themselves or can ask their fabrication partners to provide these services.

To calculate the values, the designer needs to know the following information:

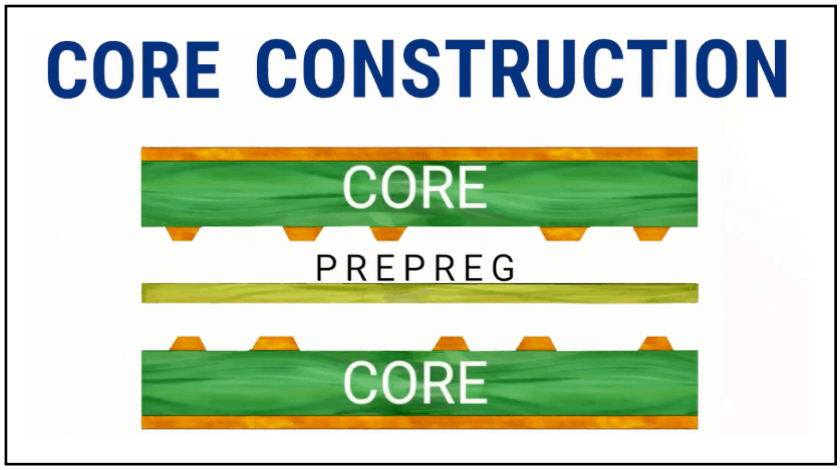
- Number of board layers
- Layers on which to route controlled impedance traces
- Layers to use as reference layers
- PCB materials used and copper thicknesses on various layers
- Dielectric constant and dielectric height (when modeling yourself, it is a good idea to use a 4-mil dielectric height for inner layers and 3mils for outer layers)

2.3 Press-out thickness

Remember, we also plan based on the press-out thicknesses that we expect from the prepreg. This is based on the amount of resin in the prepreg, the copper area, and the thickness of copper on the opposing layers. We get the copper area from the data you send us to create a final model. So, we don't follow the thickness on the datasheet. We follow our press-out thicknesses in modeling, which varies slightly from design to design. That is why, after an initial stack-up and target line widths, we come back to you for approval on small adjustments to the trace widths and spacing.

2.4 Core construction

Some customers choose to go with a core construction over a foil construction. The core construction is when we use an already cured core material for the outer layer and the next layer so that the dielectric thickness does not change after lamination. This construction takes away the variation in dielectric height. However, this type of construction or stackup is not always possible, like in HDI PCB manufacturing.



2.5 Controlled impedance and HDI PCBs

All manufacturers have a restriction on the height of copper based on the spacing requirements. Check our table below:

Minimum Trace/space required by SPE with respect to copper weight as below,

Start Copper	Minimum Capability in mils(Outer Layers)		Minimum Capability in mils(Inner Layers)	
	Line width	Space	Line width	Space
5 micron	2	3	2	2
9micron / 1/4oz	3	3	2.5	2.5
1/2 oz	4	4	3	3
1oz	6	6	4	4
2oz	8	8	6	6
3oz	12	12	7	7
4oz	14	14	8	8
5oz	16	16	9	9
6oz	20	20	10	10

This means that if you are doing HDI or have trace and space less than 3mils, you should pay attention to the copper weight at the time of modeling. If you have a blind via on that layer, then the manufacturer has to consider the aspect ratio of the blind via which should be 0.75:1 to ensure good plating in the via. So, for modeling impedance on HDI designs, the thickness of the dielectric is controlled by the aspect ratio of the microvia. Moreover, thickness is a big part of modeling.

2.6 Better tolerances for better performance

More copper weight equals more variation in the shape of the trace. Sometimes, you can even get undercut which has to be factored into the impedance modeling. So, you get better tolerances when you buy from an expert PCB manufacturer since they invest in controlling their processes better, which means better-performing circuit boards for you. Hence, it is not just the base materials; it is also how the board is processed, impacting the final performance.

2.7 Stack-up examples for 4,6, and 8-layer boards

Example of a stack-up for a 4-layer board:

4 Layer	Drills & µVias	Foil / Core / Prepreg Details	CU Oz / Th. Mils	Dk @ 10GHz	Plating Mils	4 L Cl-1	Cu %	Final Thickness
		Solder mask	0.500	4.20				0.500
4L-1		CU Foil	0.25		1.1	S	100%	1.450
		3.6 Mil Prepreg	3.600	3.63				3.348
4L-2		Copper	0.5		0	P	64%	0.700
		49 Mil Core 0.5/0.5	49	3.72				49.000
4L-3		Copper	0.5		0	P	64%	0.700
		3.6 Mil Prepreg	3.600	3.63				3.348
4L-4		CU Foil	0.25		1.1	S	100%	1.450
		Solder mask	0.500	4.20				0.500
		FINISHED PCB THICKNESS (mils)						60.996
		PCB thickness after Lamination						*57.796*
		# OF LAMINATIONS: 1						

Example of a stack-up for a 6-layer board:

6 Layer	Drills & µVias	Foil / Core / Prepreg Details	CU Oz / Th. Mils	Dk @ 10GHz	Plating Mils	4 L Cl-1	Cu %	Final Thickness
		Solder mask	0.500	4.20				0.500
6L-1		CU Foil	0.25		1.1	S	100%	1.450
		3.6 Mil Prepreg	3.600	3.63				3.348
6L-2		Copper	0.5		0	P	64%	0.700
		4 Mil Core 0.5/0.5	4.000	3.84				4.000
6L-3		Copper	0.5		0	S	24%	0.700
		41 Mil Prepreg	41.000	3.69				39.936
6L-4		Copper	0.5		0	S	24%	0.700
		4 Mil Core 0.5/0.5	4.000	3.84				4.000
6L-5		Copper	0.5		0	P	64%	0.700
		3.6 Mil Prepreg	3.600	3.63				3.348
6L-6		CU Foil	0.25		1.1	S	100%	1.450
		Solder mask	0.500	4.20				0.500
		FINISHED PCB THICKNESS (mils)						61.332
		PCB thickness after Lamination						*58.132*
		# OF LAMINATIONS: 1						

Example of a stack-up for an 8-layer board:

8 Layer	Drills & µVias	Foil / Core / Prepreg Details	CU Oz / Th. Mils	Dk @ 10GHz	Plating Mils	8 L Cl-1	Cu %	Final Thickness
		Solder mask	0.500	4.20				0.500
8L-1		CU Foil	0.25		1.1	S	100%	1.450
		3.6 Mil Prepreg	3.600	3.63				3.348
8L-2		Copper	0.5		0	P	64%	0.700
		4 Mil Core	4.000	3.84				4.000
8L-3		Copper	0.5		0	S	24%	0.700
		7.2 Mil Prepreg	7.200	3.63				6.416
8L-4		Copper	0.5		0	P	64%	0.700
		28 Mil Core	28.000	4.24				28.000
8L-5		Copper	0.5		0	P	64%	0.700
		7.2 Mil Prepreg	7.200	3.63				6.416
8L-6		Copper	0.5		0	S	24%	0.700
		4 Mil Core	4.000	3.84				4.000
8L-7		Copper	0.5		0	P	64%	0.700
		3.6 Mil Prepreg	3.600	3.63				3.348
8L-8		CU Foil	0.25		1.1	S	100%	1.450
		Solder mask	0.500	4.20				0.500
		FINISHED PCB THICKNESS (mils)						63.628
		PCB thickness after Lamination						*60.428*
		# OF LAMINATIONS: 1						

2.8 Common mistakes to avoid in the stack-up boards

2.8.1 Prepregs

It is recommended not to use more than three different types of prepregs in a stack-up. Furthermore, the dielectric thickness of each prepreg layer should be less than 10mils; otherwise it will increase the chance of a greater variation in the final thickness. You should avoid using prepregs with very low resin and high glass content: very low resin content may lead to resin starvation during lamination.

Very low resin and high glass content prepregs use 7628 and 2116 content glass styles. 2113 glass style is a borderline case. If possible, avoid it in a prepreg layer unless there are no adjoining copper layers.

2.8.2 Impedance trace/space

It is a good design practice that the spacing between the two traces of a differential pair should not be more than twice the width of the traces. For instance, a 4-mil differential trace should not have more than an 8-mil space. As often as possible, the trace width should not exceed twice the dielectric thickness between the target signal layer and the nearest reference layer.

2.8.3 How to calculate the average effective dielectric constant

When there are several types of dielectric materials (having different dielectric constants) between the signal layer and the reference plane, it becomes necessary to calculate the effective dielectric constant of this composite dielectric material. A simple way is to calculate the weighted average of the dielectric constant as stated below:

$$\text{DK effective} = \frac{\text{Type 1 (thickness of material) x (DK value)} + \text{Type 2 (thickness of material) x (DK value)}}{\text{(thickness of material type 1 + type 2)}}$$

Ex: 370 HR		thickness (in mils)	DK
signal layer	foil		
prepreg	2 x 106 (type of prepreg)	2 x 2.3 = 4.6 mils	3.22
core	8 mils	1 x 8 = 8 mils	3.65
reference layer			

$$\text{DK effective} = \frac{(4.6 \times 3.22) + (8 \times 3.65)}{(4.6 + 8)} = \frac{(14.812) + (29.2)}{(12.6)} = 3.49$$

2.8.4 High-speed materials

High-speed materials are materials suitable for applications that require the transmission of high-speed signals (500MHz to 3GHz). Some of the high-speed materials that Sierra Circuits uses are given below:

- Isola FR408HR
- Isola I-Speed
- Isola I-Tera MT40
- Panasonic Megtron6
- Rogers (like RO4350, RO3003, etc.)

Most high-speed materials are characterized by low values of the dielectric constant and dissipation factor compared to the most commonly used FR4 type PCB material, like 370 HR or Ventec VT47.

2.9 Why manufacturers change your trace width and spacing?

Ask yourself: is the material you need available in the thickness that you require? Common core dielectric thicknesses are 3mils, 4mils, 5mils, 6mils, 8mils, etc. Common prepreg glass styles are 106, 1080, etc. See the thickness and the dielectric constant of the generic prepreg glass styles in the table in section 2.1.

The thickness of the material is found on the material data sheets or is available from the laminate manufacturers. PCB manufacturers calculate the final press-out thicknesses that they expect from the prepreg, which depends on the amount of resin in the prepreg, the amount of the copper area percentage, and the thickness of the adjoining copper layers. PCB manufacturers calculate the copper area percentage from the CAD files that you sent. Therefore, they do not follow the generic thickness specified on the datasheets. They follow their press-out thicknesses for impedance modeling, which will change from design to design. This will require small adjustments in the trace widths and spacing of the controlled impedance traces. If the manufacturers cannot meet the impedance requirement that you are looking for with the dielectric thicknesses or material types you have selected, they will suggest an alternative dielectric thickness or PCB material.

3. How to design a board with controlled impedance

3.1 Determining which signals require controlled impedance

PCB designers have to follow strict guidelines for controlled impedance when designing the board. Most of the time, electrical engineers specify which signal nets require a specific controlled impedance. However, if they do not, the designer should review the datasheets of the integrated circuits to determine which signals require controlled impedance. The datasheets usually provide detailed guidelines for each group of signals and their impedance values. The spacing rules and information on which layer to route specific signals may also appear in the datasheets or in the application notes. DDR traces, HDMI traces, Gigabit Ethernet traces, RF signals are some of the examples of controlled impedance traces.

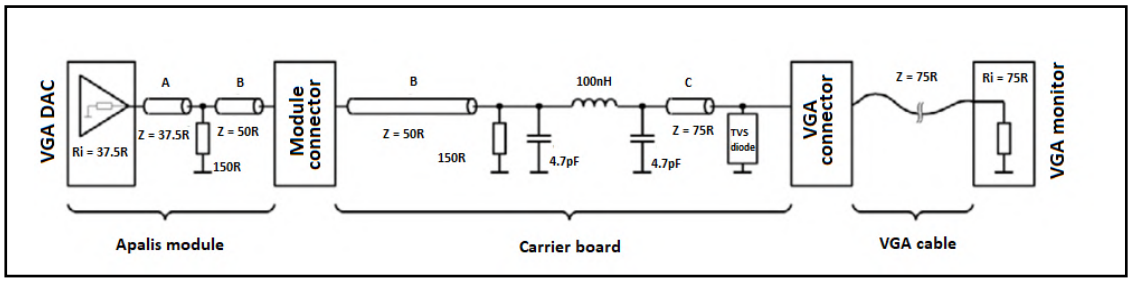
3.2 Impedances of some standard communication interfaces

The following table gives certain standard communication interfaces and their specific impedance values.

Impedance for various interfaces:

	Type of Interface	Differential Impedance	Single Ended Impedance
1	PCI Express	90Ω ±15%	50Ω ±15%
2	SATA	90Ω ±15%	55Ω ±15%
3	Ethernet	95Ω ±15%	55Ω ±15%
4	USB 2.0 Signals	90Ω ±15%	50Ω ±15%
5	USB 3.0 Signals	90Ω ±15%	50Ω ±15%
6	Parallel RGB LCN	N/A	50Ω ±15%
7	LVDS LCD	100Ω ±15%	55Ω ±15%
8	HDMI/DVI	90Ω ±15%	50Ω ±15%
9	Analogue VGA	N/A	50Ω ±15% section B 75Ω ±15% section C See Figure Below
10	Parallel Camera Interface	N/A	50Ω ±15%
11	SD/MMC/SDIO	N/A	50Ω ±15%
12	I2C	N/A	50Ω ±15%
13	Display Serial Interface (MIPI/DSI with D-PHY)	90Ω ±15%	50Ω ±15%
14	Camera Serial Interface (MIPI/CSI-2 with D-PHY)	90Ω ±15%	50Ω ±15%

Here are some examples of schematics properly annotated with impedance values:

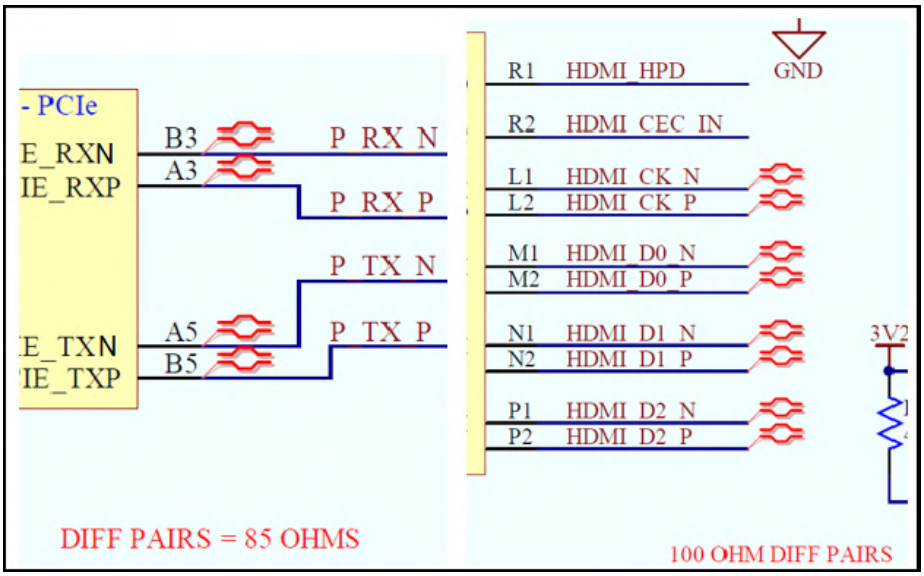


VGA signal trace impedance sections

3.3 Annotate the schematic with impedance requirements

The design of a board starts with the design of the circuit schematics by the design engineer. The engineer must specify controlled impedance signals in the schematic and classify specific nets to be either differential pairs (100Ω, 90Ω or 85Ω) or single-ended nets (40Ω, 50Ω, 55Ω, 60 Ω or 75Ω). It's a good design practice to add N or P polarity indication after the net names of the differential pair signals in a schematic. The engineer should also specify particular controlled impedance lay-out design guidelines (if any) to be followed by the layout designer, either in the schematic or in a separate "Read Me" file.

In this Altium schematic, the differential pairs have appropriate net names:



3.4 Determine the trace parameters for controlled impedance

A PCB trace is defined by its thickness, height, width, and dielectric constant (Er) of the material on which the traces are etched. While designing controlled impedance boards, it is essential to take care of these parameters. You can provide the manufacturer with the number of layers, the value of the impedance traces on specific layers (50Ω, 100Ω on layer 3), and materials for PCB designing.

The manufacturer gives you the stack-up that mentions the trace widths on each layer, the number of layers, the thickness of each dielectric in the stack-up, trace thickness, and PCB material. They also take care of the controlled impedance requirements by calculating the feasible thickness, width, and height for the traces that need impedance control. Stick to the following relationships to know how impedance depends on dimensions:

- Impedance is inversely proportional to trace width and trace thickness.
- Impedance is proportional to the laminate height, and it is inversely proportional to the square root of the laminate's dielectric constant (Er).

3.5 Common mistakes to avoid when designing for controlled impedance

3.5.1 Distinguishing controlled impedance traces from other traces

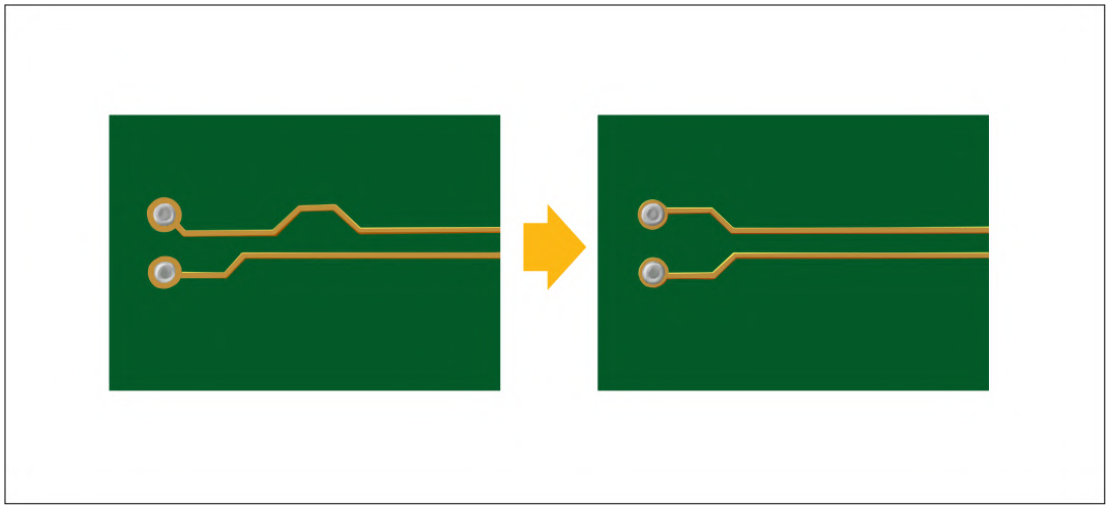
The controlled impedance trace widths must be distinguishable from the remaining traces in the board. This allows the PCB manufacturer to easily identify them and make suitable changes to the trace width if necessary to achieve a certain impedance. For example, suppose you require a 5-mil trace to achieve 50-ohm impedance, and you have also routed other signals with 5 mil width. In that case, it will be impossible for the PCB manufacturer to determine which ones of these are the controlled impedance traces. Therefore, you should make the 50-ohm impedance traces 5.1-mil or 4.9-mil wide.

The table below shows trace widths and spacings for controlled impedance on different layers. Non-impedance signal traces should not be routed with 3.5, 3.6, 4.2, 4.25, and 4.3-mil trace widths.

Layer	50Ω (SE)	Differential pair 90 ohms		Differential pair 100 ohms	
		90Ω Trace	90Ω Space	100 Ohm Trace	100Ω Space
1	4.3 mils	4.25 mils	6.25 mils	3.5 mils	7 mils
3	4.2 mils	4.4 mils	6.1 mils	3.6 mils	6.9 mils
6	4.2 mils	4.4 mils	6.1 mils	3.6 mils	6.9 mils
8	4.3 mils	4.25 mils	6.25 mils	3.5 mils	7 mils

3.5.2 Maintain symmetry in differential pair routing

High-speed differential pair signal traces need to be routed parallel to each other with a constant spacing between them. The specific trace width and the spacing are required to calculate the particular differential impedance. The differential pairs need to be routed symmetrically. You should minimize areas where the specified spacing is enlarged due to pads or the ends.



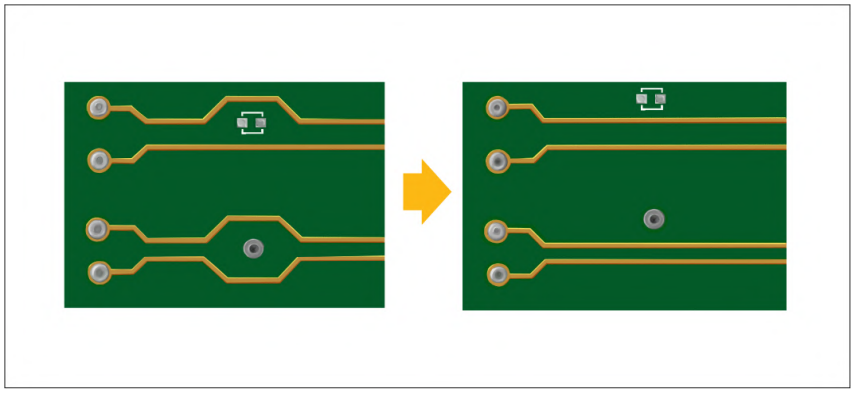
Route differential pairs symmetrically and keep signals always parallel.

3.5.3 Adequate spacing between controlled impedance traces, other traces, and components (3W and 2W rule)

To reduce crosstalk, the spacing between traces should be 3W or a minimum of 2W. Note that this rule does not apply to the spacing between differential pairs.

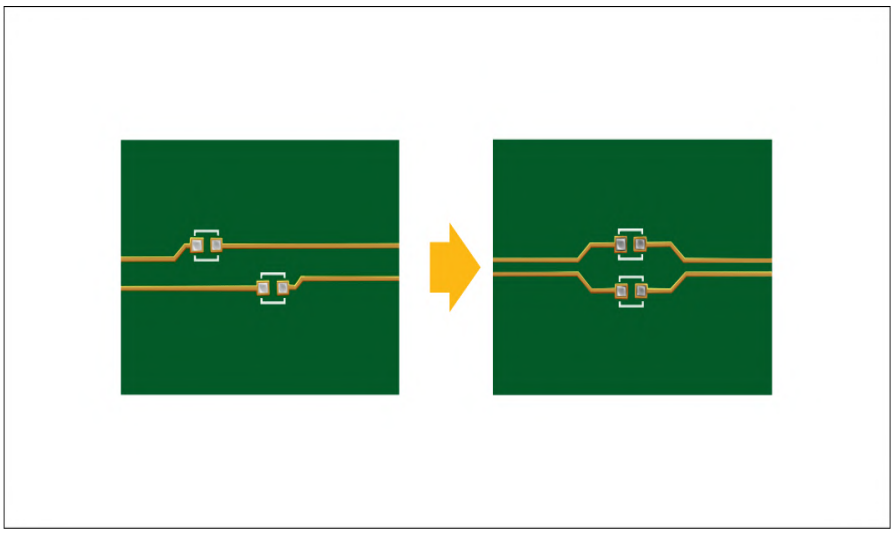
3.5.4 Placement of components, vias, and coupling capacitors

Components or vias should not be placed between differential pairs, even if the signals are routed symmetrically around them. Components and vias create a discontinuity in impedance and could lead to signal integrity problems. For high-speed signals, the spacing between one differential pair and an adjacent differential pair should not be less than five times the width of the trace (5W). You should also maintain a keep-out of 30mils to any other signals. For clocks or periodic signals, you should increase the keep-out to 50mils to ensure proper isolation.



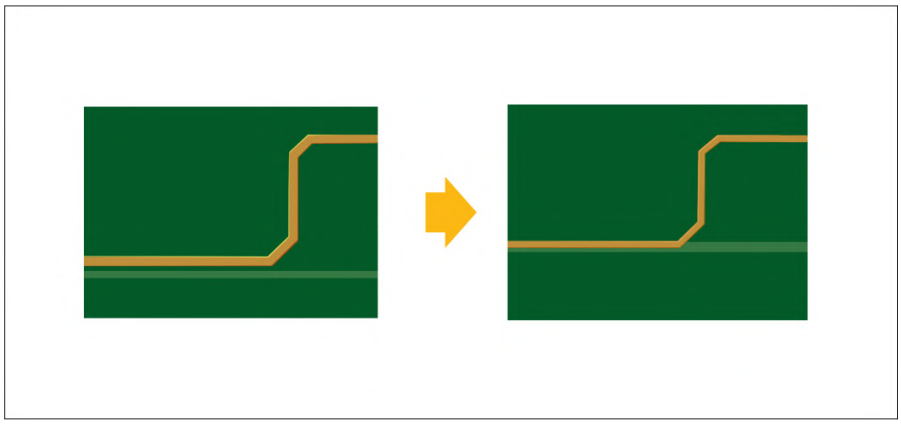
Avoid components and vias between differential pairs.

If high-speed differential pairs require serial coupling capacitors, they need to be placed symmetrically, as shown in the below figure. The caps create impedance discontinuities, so placing them symmetrically will reduce the amount of discontinuity in the signal.



Place coupling capacitors symmetrically to avoid discontinuities.

You should minimize the use of vias for differential pairs, and if you do place them, they need to be symmetrical to minimize discontinuity.

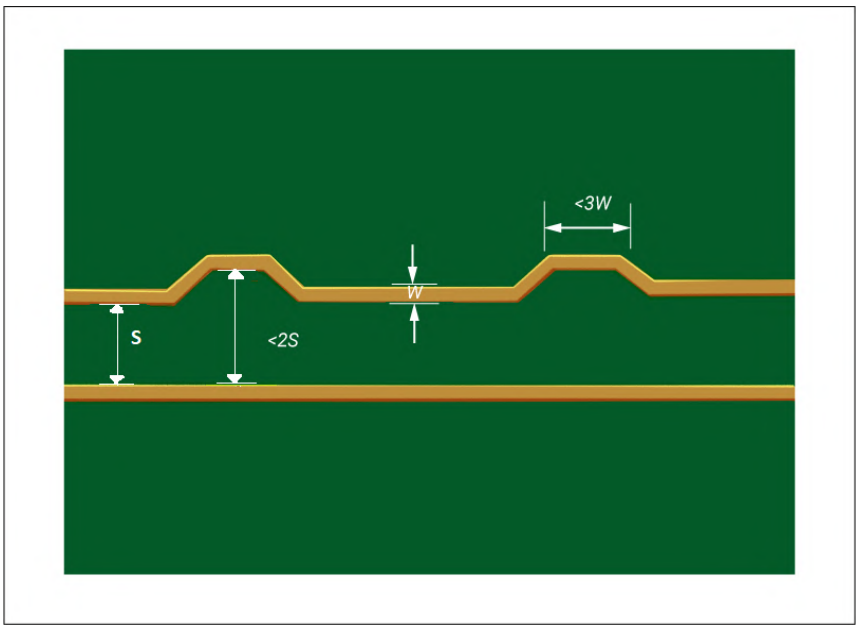


Do not route high-speed signals at plane and PCB borders.

3.5.5 Length matching

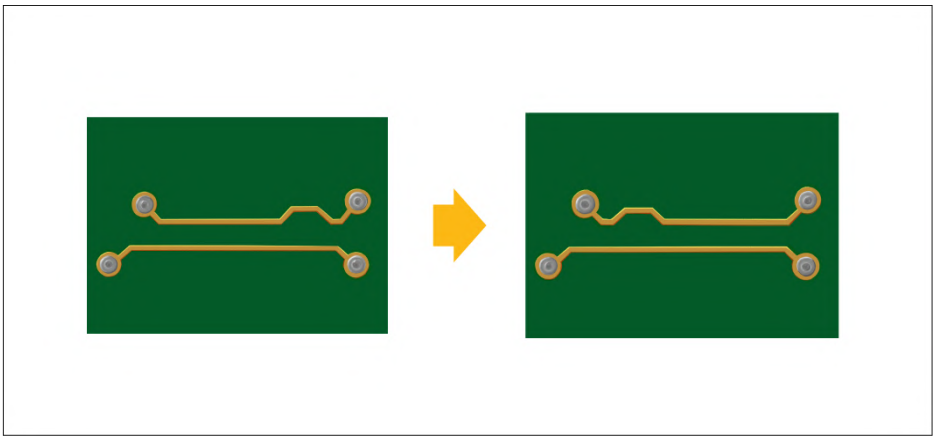
Length matching will achieve propagation delay matching if the speed of the signals on various traces is the same. Length matching may be required when a group of high-speed signals travel together and are expected to reach their destination simultaneously (within a specified mismatch tolerance).

The lengths of the traces forming a differential pair need to be matched very closely; otherwise, that would lead to an unacceptable delay skew (mismatch between the positive and negative signals). The mismatch in length needs to be compensated by using serpentines in the shorter trace. The geometry of serpentine traces needs to be carefully chosen to reduce impedance discontinuity. The figure below shows the requirements for ideal serpentine traces.



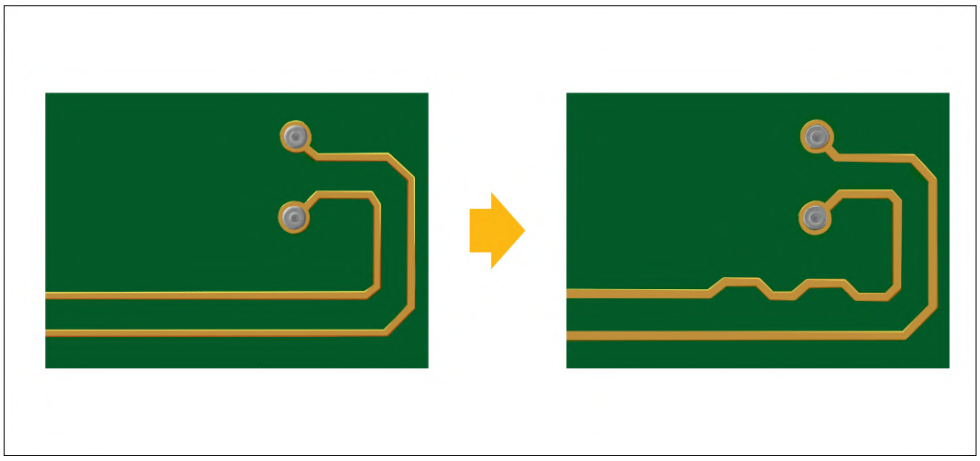
Length matching for propagation delay reduction.

The serpentine traces should be placed as near as possible to the source of mismatch. It ensures the mismatch correction as soon as possible. In the figure below, you can see that the mismatch occurs on the left set of vias, so the serpentine needs to be added on the left rather than on the right.



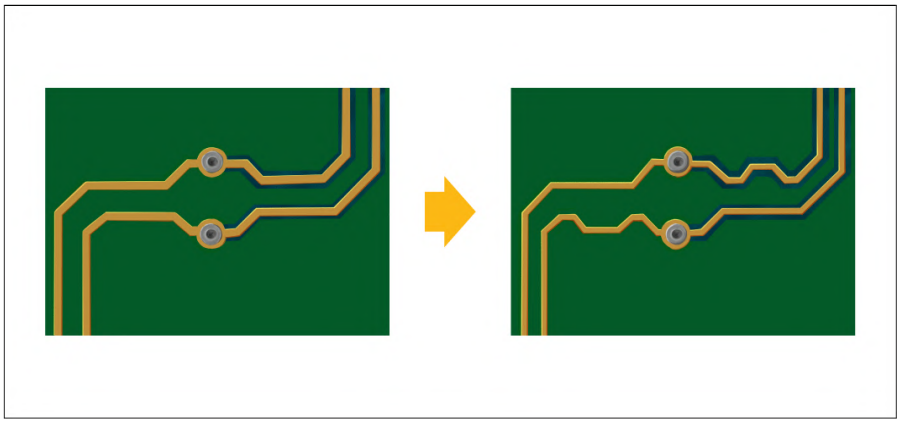
Length correction to the mismatching point.

Similarly, bends cause mismatching making the trace on the inner bend smaller than the outer trace. Therefore, we need to add serpentines as close to the bend area. If a pair has two bends closer than 15mm, they compensate each other. Hence you do not need to add serpentines.



Length compensation close to the bend.

When a differential pair signal changes from one layer to another using vias and has a bend, each segment of the pair needs to be matched individually. Serpentines should be placed on the shorter traces near the bend. You need to manually inspect for this violation as it will not be caught in Design Rule Checks since the lengths of the total signals will be closely matched. Since the signal speed of traces on various layers may be different, it is recommended to route differential pair signals on the same layer if they require length matching.

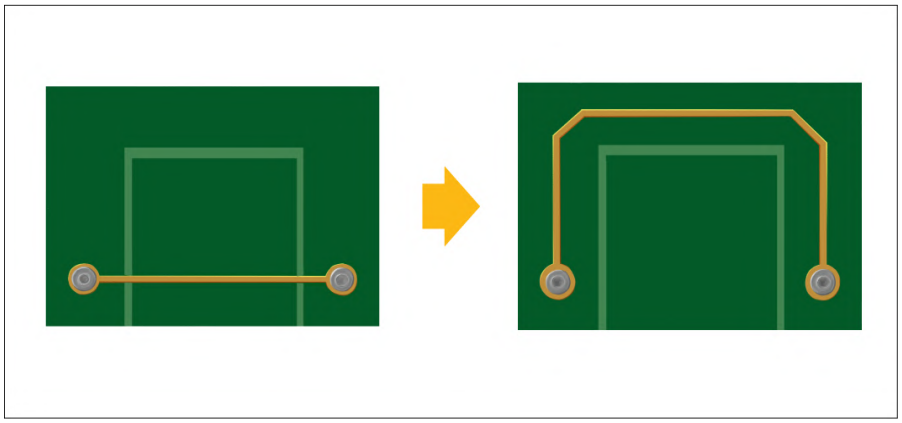


Length differences need to be compensated in each segment.

3.5.6 Reference layers for the return path of controlled impedance signals

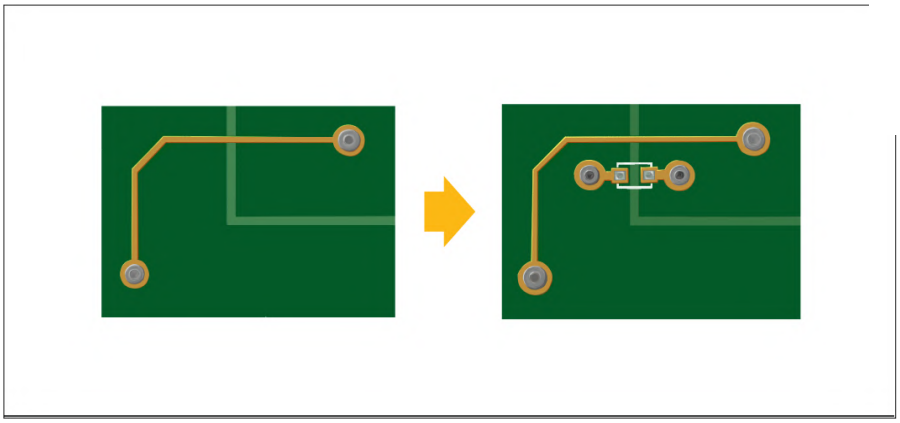
All high-speed signals require a continuous reference plane for the return path of the signal. An incorrect signal return path is one of the most common sources for noise coupling and EMI issues. The return current for high-speed signals closely follows the signal path, whereas the return current for low-speed signals takes the shortest path available. Generally, the return path for high-speed signals is provided in the reference planes nearest to the signal layer.

High-speed signals should not be routed over a split plane because the return path will not be able to follow the trace. You should route the trace around the split plane for better signal integrity. Also, ensure that the ground plane is a minimum of three times the trace width (3W rule) on each side.

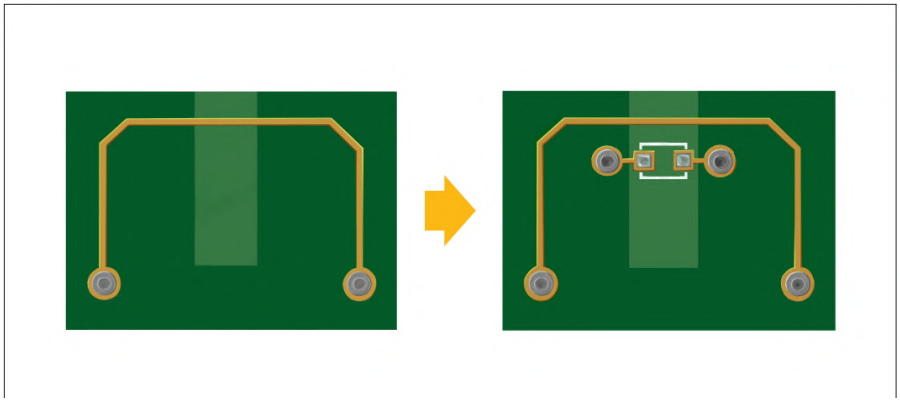


Avoid routing over split planes.

A stitching capacitor between the two reference planes is required if a signal needs to be routed over two different reference planes. The capacitor needs to be connected to the two reference planes and should be placed close to the signal path to keep the distance between the signal and the return path small. The capacitor allows the return current to travel from one reference plane to the other and minimizes impedance discontinuity. A good value for the stitching capacitor is between 10nF and 100nF.



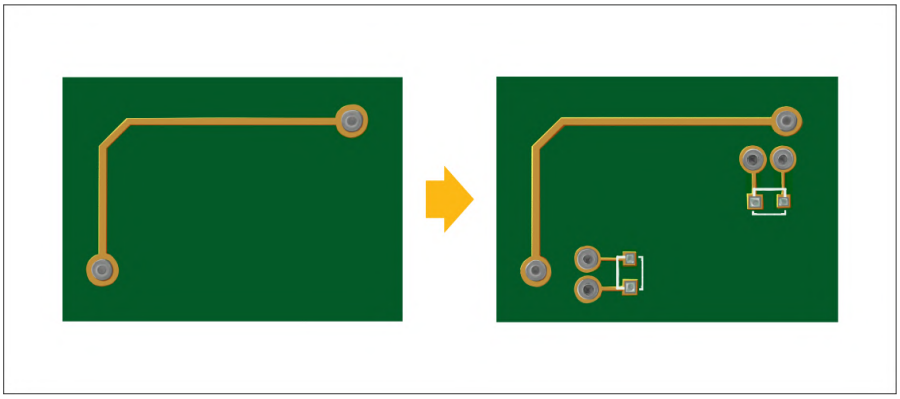
You should avoid both split plane obstructions and slots in the reference plane just underneath the signal trace. If the slots are unavoidable, stitching vias should be used to minimize the issues created by the separated return path. Both pins of the capacitor should be connected to the ground layer and should be placed near the signal.



Stitching capacitor needed when routing over plane obstructs.

When vias are placed together, they create voids in reference planes. To minimize these large voids, you should stagger the vias to allow sufficient feed of the plane between vias. Staggering the vias allows the signal to have a continuous return path.

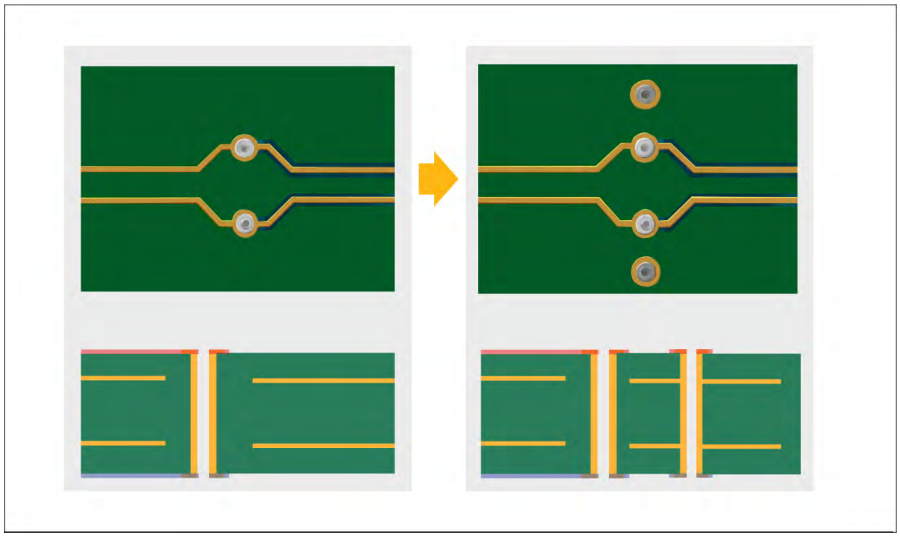
It is preferred to use ground planes for reference. However, if a power plane is used as a reference plane, you need to add a stitching capacitor to allow the signal to change the reference from the ground to the power plane and then back to the ground. You should place a capacitor close to the signal entry and exit points and connect one end to the ground and the other to the power net.



Add stitching capacitors when using power planes as reference.

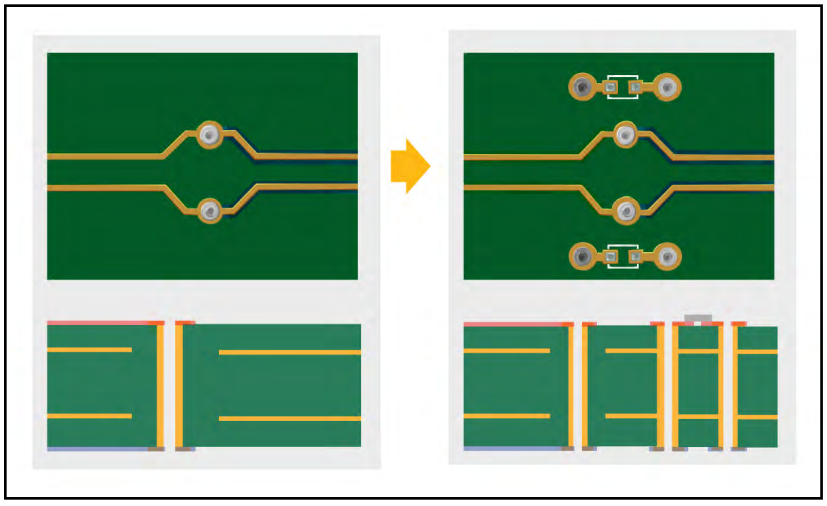
3.5.7 Add stitching vias close to the layer change vias

If a high-speed differential pair or single-ended signal switches layers, you should add stitching vias close to the layer change vias. This practice also allows the return current to change ground planes.



Place stitching vias when the signal changes ground reference.

Suppose a high-speed signal trace switches to a layer with a different net as reference. In that case, stitching capacitors are required to allow the return current to flow from the ground plane through the stitching capacitor to the power plane. The placement of the capacitors should be symmetrical for differential pairs.



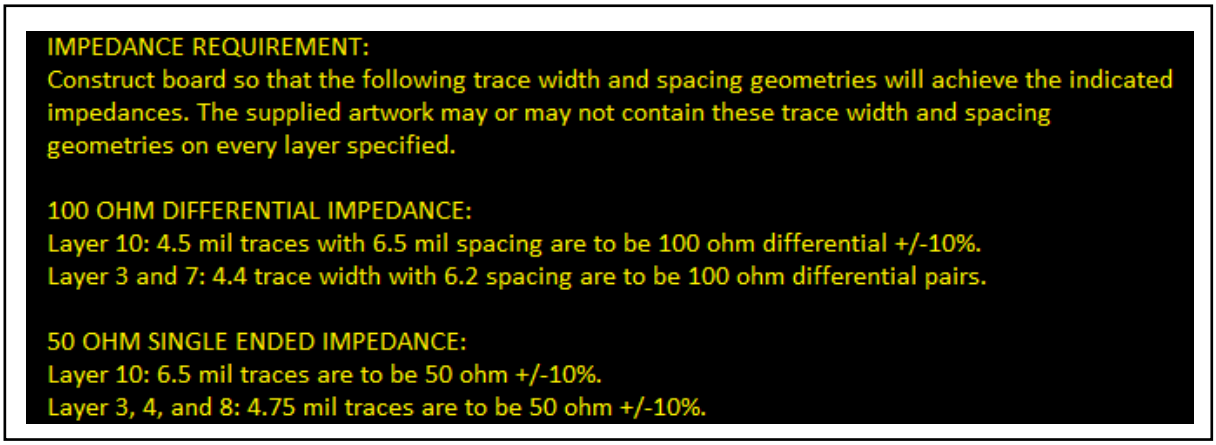
Place stitching capacitor when changing signal reference plane.

3.6 How to document controlled impedance requirements in PCB design?

A layout designer must include the impedance information in the fabrication drawing notes and tables. The information should include the impedance value, the trace width, the spacing for differential pairs, and the layer on which the controlled impedance traces are routed. Preferably, an impedance table should be provided in the fabrication drawing. Here is an example of a table:

LAYER	50 OHM	100 OHM	
	Trace	Trace	Space
3	4.75 Mils	4.40 Mils	6.20 Mils
4	4.75 Mils		
7		4.40 Mils	6.20 Mils
8	4.75 Mils		
10	6.50 Mils	4.50 Mils	6.50 Mils

The figure below provides an example of how to specify controlled impedance on a fabrication drawing:



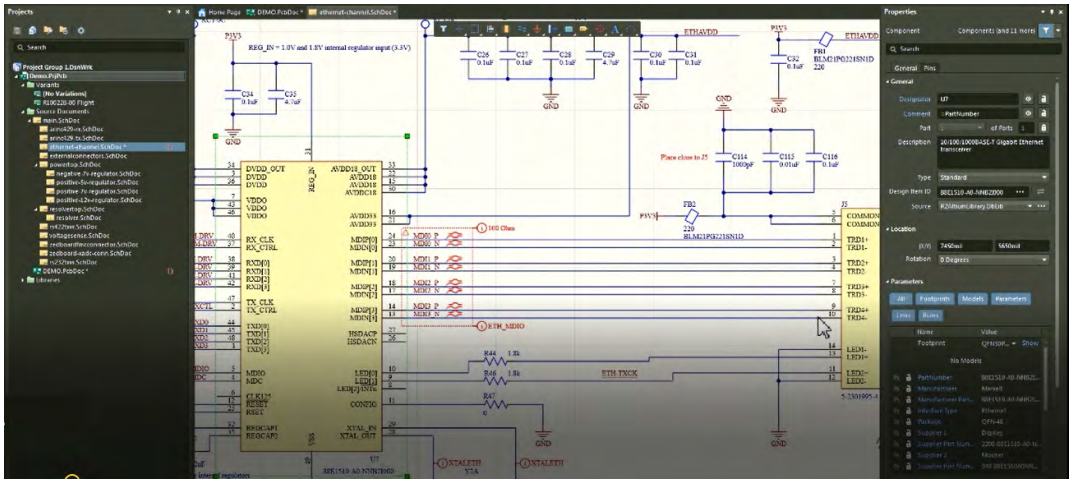
The PCB manufacturer will review these notes and create a stackup to get the desired trace width and spacing specified in the notes. They can make minor adjustments in the trace width and spacing to achieve the desired impedance.

4. Controlled impedance routing using Altium Designer

In this chapter, we will demonstrate controlled impedance routing using Altium Designer. Let's take you through the following steps to achieve the desired impedances for single-ended and differential traces using Altium Designer.

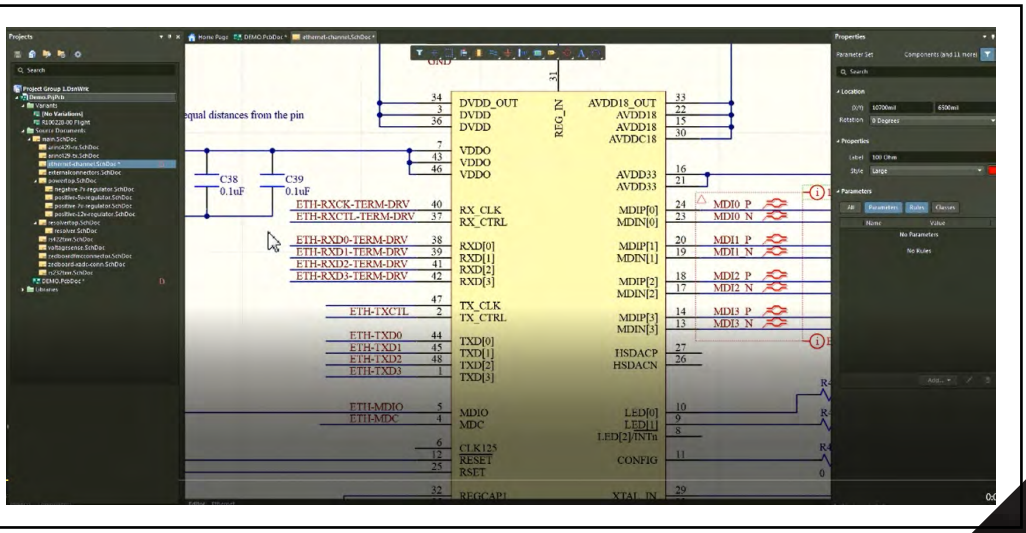
In this demo, we will show you how to route the differential pair with 100 ohms and a single-ended line with 50 ohms. Here, this is the ethernet section with ethernet IC and RJ45 connector.

Check out the complete tutorial **here.**



Ethernet section with ethernet IC and RJ45 connector.

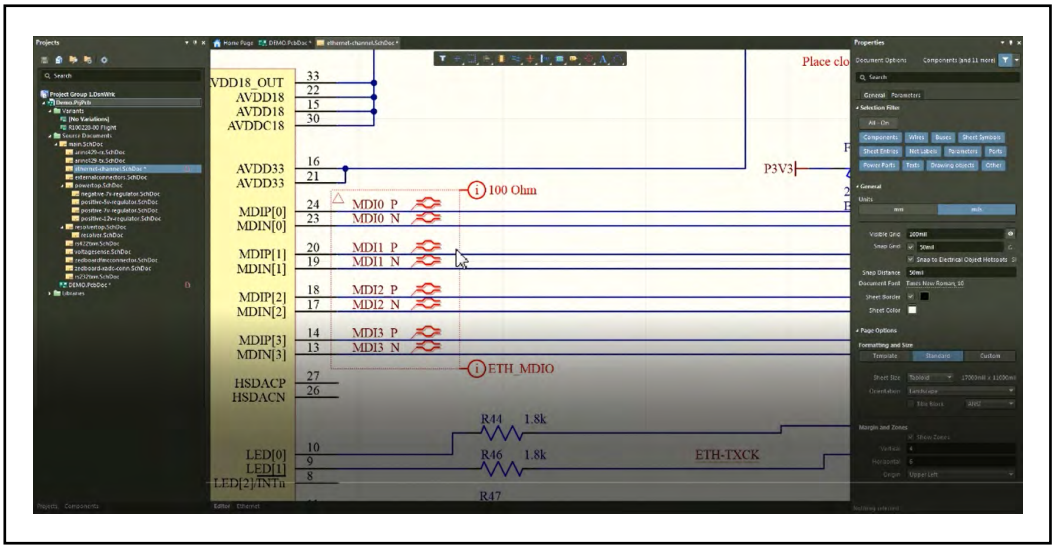
You can see the net with the **receiver (RX) and transmitter (TX) section, RX clock, RX control, and RXD0, D1, D2, and D3.** These all are single-ended **50-ohm** traces.



A net with the receiver (RX) and transmitter (TX) section.

4

On another side of the IC, you can see an **MDI0, one, two, and three**. All these connections are 100-ohm differential pairs.



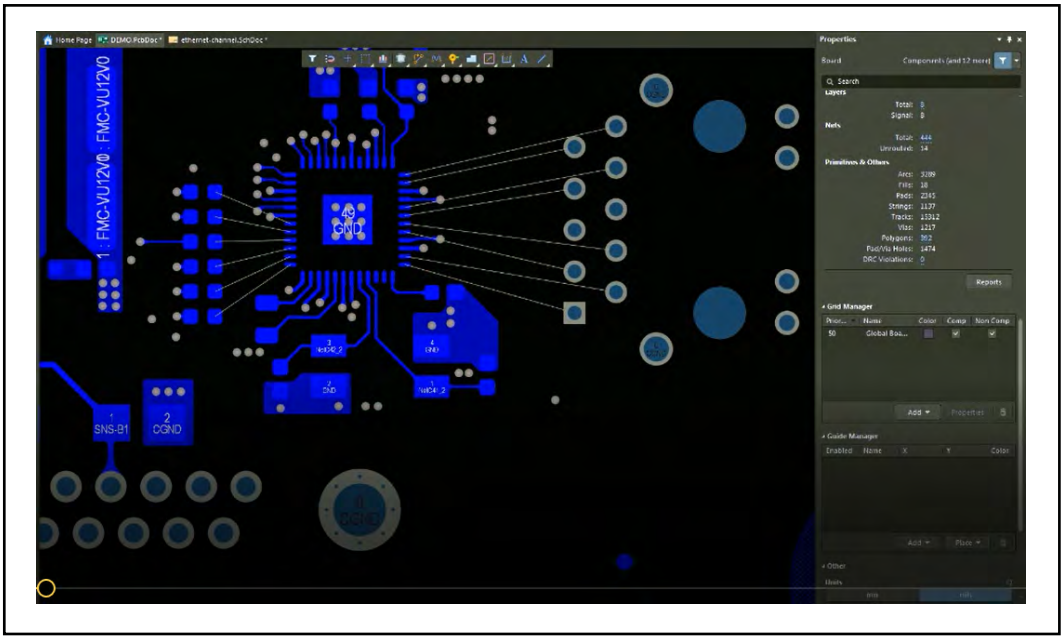
To achieve the impedances, we need certain trace widths; those will be provided by the manufacturer in the form of a stack-up. The image given below is depicting an example of a stack-up. In this stack-up, the layers are given, the required impedances are given, and the trace width and spacing between the traces are also given.

6 Lay	Drills & µVias	Foil, Core or Prepreg Details	CU Oz / Th. Mils	Dk (10Ghz)	Plating Mils	6 L CI-1	Cu %	Final Thickness
		Solder mask	0.500	4.20				0.500
6L-1		CU Foil	0.25		1.1	S	100%	1.450
		4 Mil Prepreg	4.000	3.86				3.496
6L-2		Copper	1		0	P	64%	1.400
		5 Mil Core 1/1	5.000	3.84				5.000
6L-3		Copper	1		0	S	24%	1.400
		36 Mil Prepreg	36	4.16				33.872
6L-4		Copper	1		0	S	24%	1.400
		5 Mil Core 1/1	5.000	3.84				5.000
6L-5		Copper	1		0	P	64%	1.400
		4 Mil Prepreg	4.000	3.86				3.496
6L-6		CU Foil	0.25		1.1	S	100%	1.450
		Solder mask	0.500	4.20				0.500
		FINISHED PCB THICKNESS						60.364
		PCB thickness after Lamination						*57.164*
		# of Laminations: 1						

Impedance Models Examples

Signal layer	Ref_1 layer	Ht to Ref_1	Ref_2 layer	Ht to Ref_2	40 Ω SE	45 Ω SE	50 Ω SE	55 Ω SE	60 Ω SE	75 Ω Diff.		80 Ω Diff.		90 Ω Diff.		100 Ω Diff.		120 Ω Diff.	
					T	T	T	T	T	T	S	T	S	T	S	T	S	T	S
6L-L1	6L-L2	3.50	--	--	8.60	6.90	5.60	4.50	3.60			5.75	4.25	4.80	5.20	4.00	6.00	3.00	11.00
6L-L6	6L-L5	3.50	--	--						6.70	4.30	6.10	4.90	5.10	5.90	4.20	6.80		
All Impedances Applicable for 6L-L1 and 6L-L6										7.10	4.90	6.50	5.50	5.40	6.60	4.40	7.60		
										7.70	6.30	7.00	7.00	5.80	8.20	4.70	9.30		
6L-L3	6L-L2	5.00	6L-L5	41.66	10.70	8.60	6.80	5.50	4.40			5.80	4.20	4.80	5.20	3.90	6.10	3.00	9.70
6L-L4	6L-L5	5.00	6L-L2	41.66						6.80	4.20	6.20	4.80	5.20	5.80	4.20	6.80		
All Impedances Applicable for 6L-L3 and 6L-L4										7.30	4.70	6.70	5.30	5.50	6.50	4.50	7.50		
										8.20	5.80	7.40	6.60	6.10	7.90	4.90	9.10		

4.1 Class creation



Classes for 50 and 100-ohm traces.

- **Go to Design >> Classes >> Net classes.**

4

- Right-click **on Net classes >>** click on **Add classes.**

- Give this class a name (100 ohms in our case).

- Go to this 100-ohm class and select the nets which are there in this class and click on the arrow (**>**).

- In this way, all the nets in the class will get assigned to 100-ohm traces.

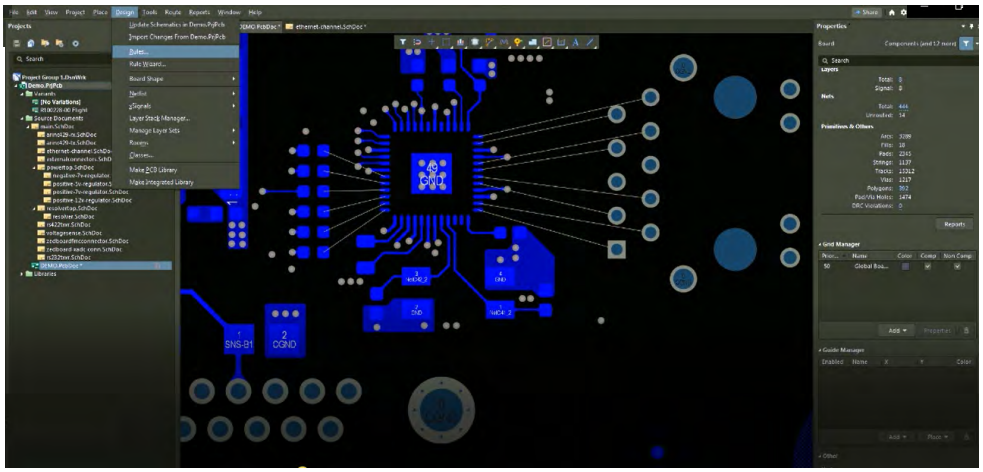
Note: In the same way we will create a **50-ohm** class.

4.2 Rule setup

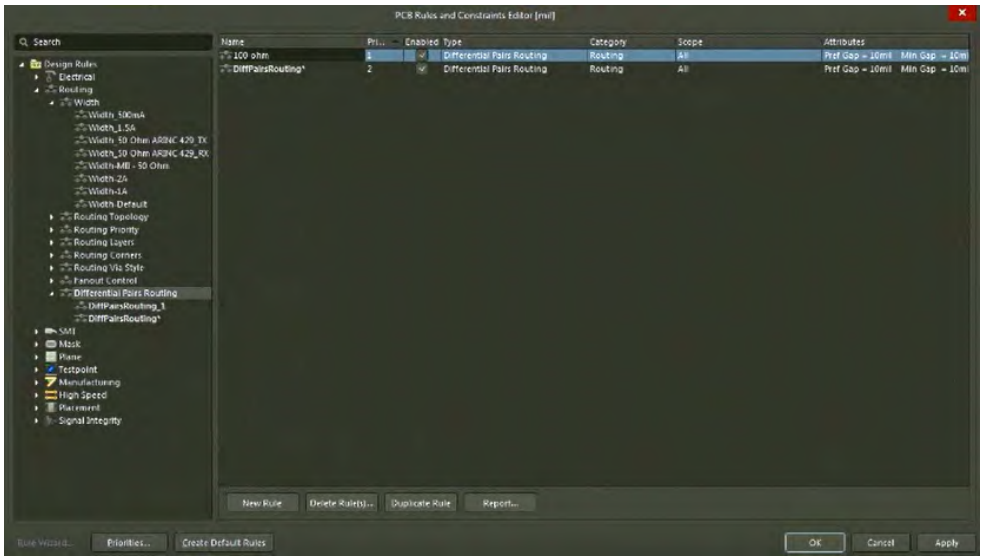
4.2.1 Rule setup for a differential pair (100 ohms)

To set the rules for the classes we created above, we will follow these steps:

- Go to **Design >> Rules**.



- Go to the **Differential pair rules >> New rule.**
- Give a name to this rule (100 ohms in this case) and double-click.

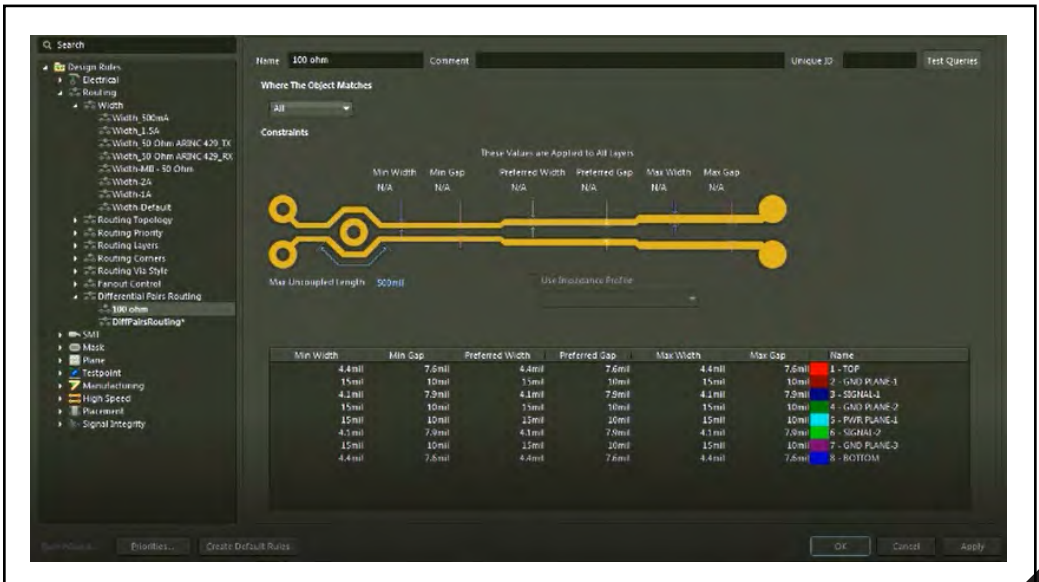


- We will now put the values for the top layer, bottom layer, signal one, and signal two. For the top layers in our stack-up, the values are 4.4mils and 7.6mils.

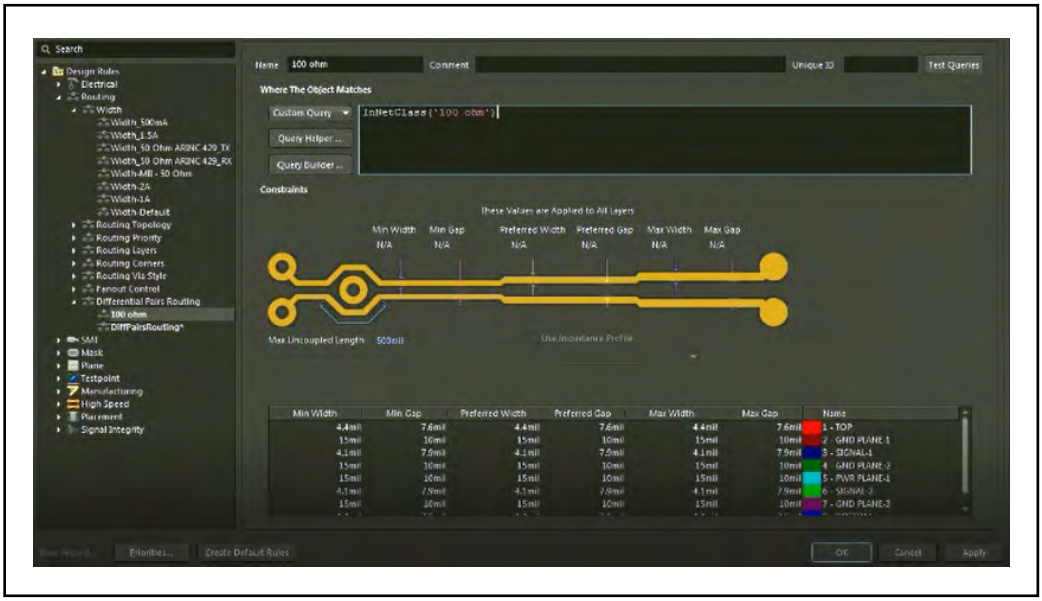
- Add minimum width, preferred width, and max-width. The minimum width will be 4.4mils, and the minimum gap will be 7.6mils.

- The impedances are dependent on the trace width and the spacing. Once we do this, we will again go to the stack-up and cross verify the signal one and signal two values. Signal one and signal two values are 4.1mils and 7.9mils.

- Add signal one and signal two values. And go to the drop-down box and select a custom query.



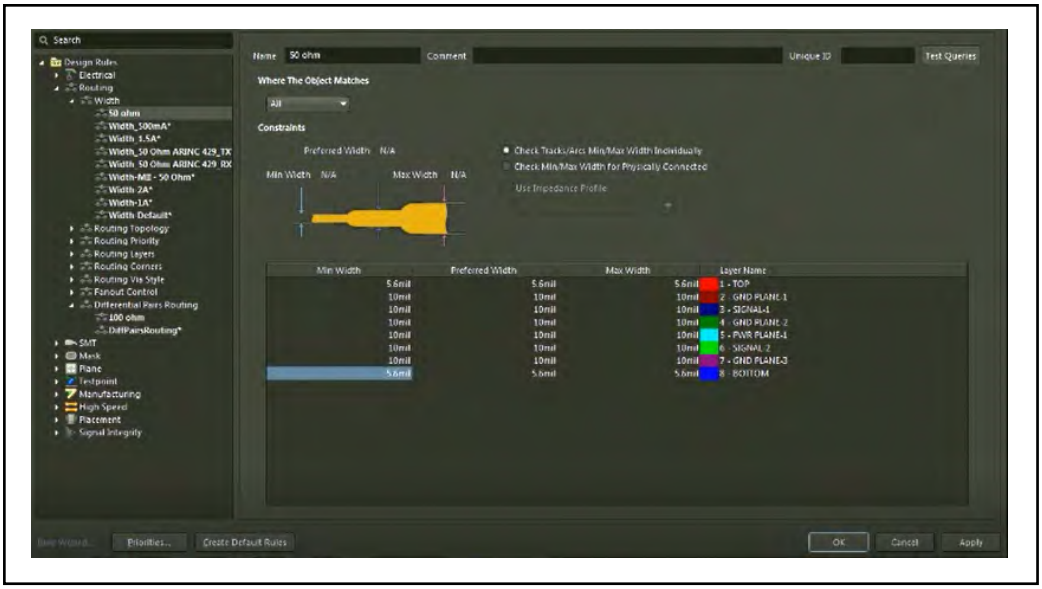
- In the drop-down box, type Net Class and select 100ohms.



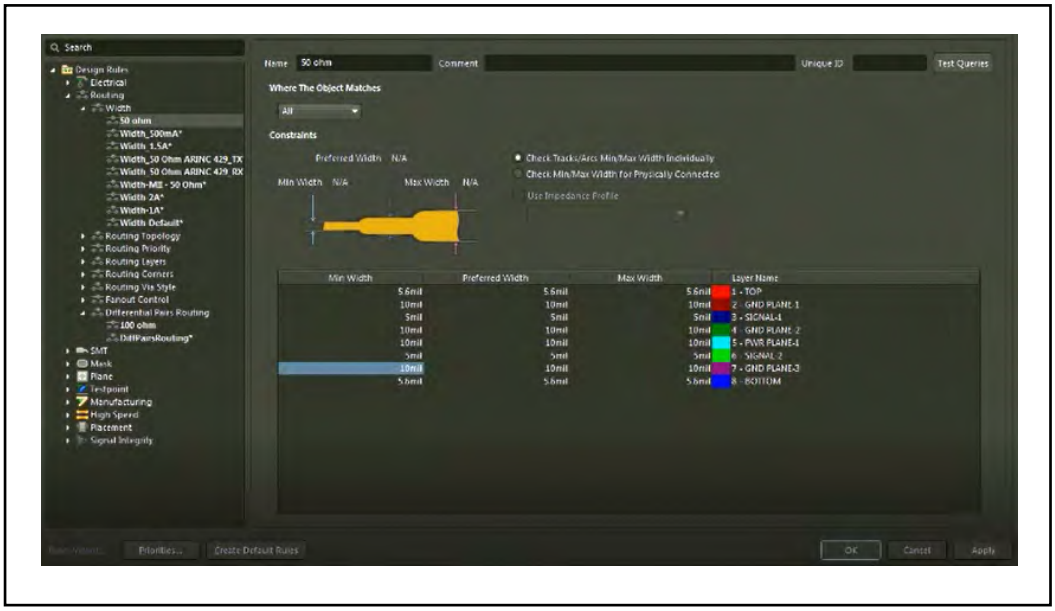
Note: The values in the top layer and the bottom layer will be the same. The ground plane and the power planes are not to be used.

4.2.2 Rule setup for a single-ended (50 ohms) line

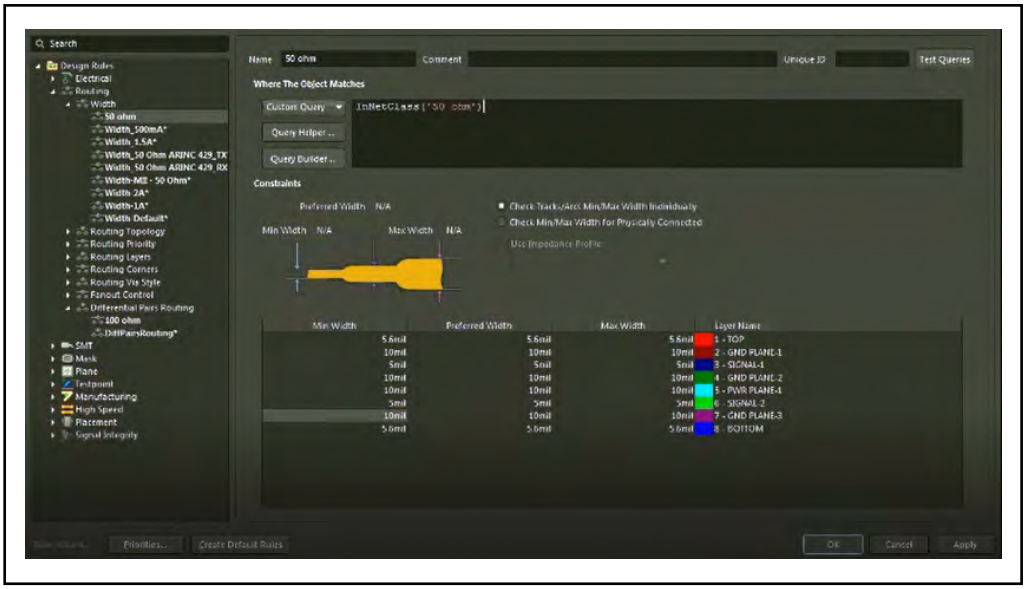
- Go to **Design >> Rules**.
- Go to the **single-ended rules >> New rule**.
- Give a name to this rule (50ohms in this case) and double-click.
- We will now put the values for the top layer, bottom layer, signal one, and signal two. For the top layer in our stack-up, the value is 5.6mils.
- Add minimum width, preferred width, and max-width that is 5.6mils.



- Go to the stack-up and add the signal one and signal two values that is 5mils.



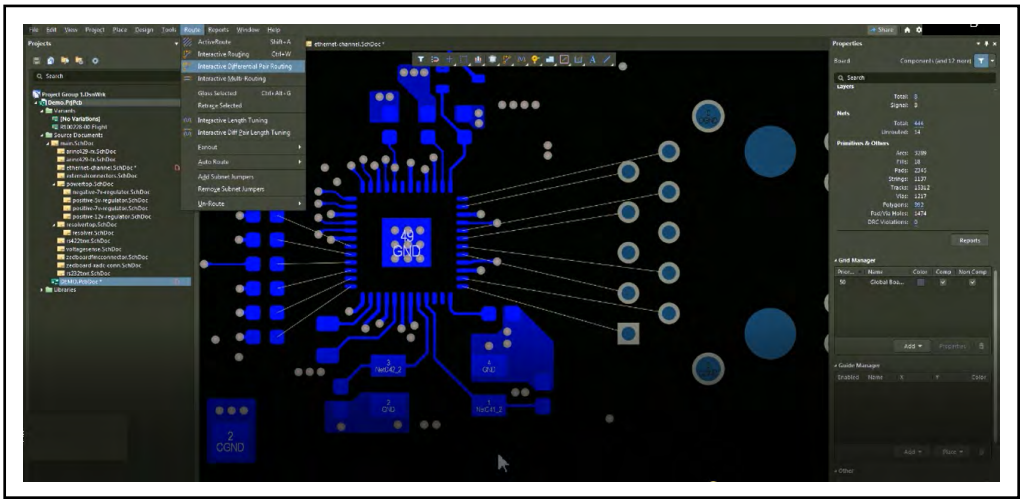
- Go to the drop-down box and select a custom query.
- In the drop-down box, type **Net Class** and select **50 ohms**.



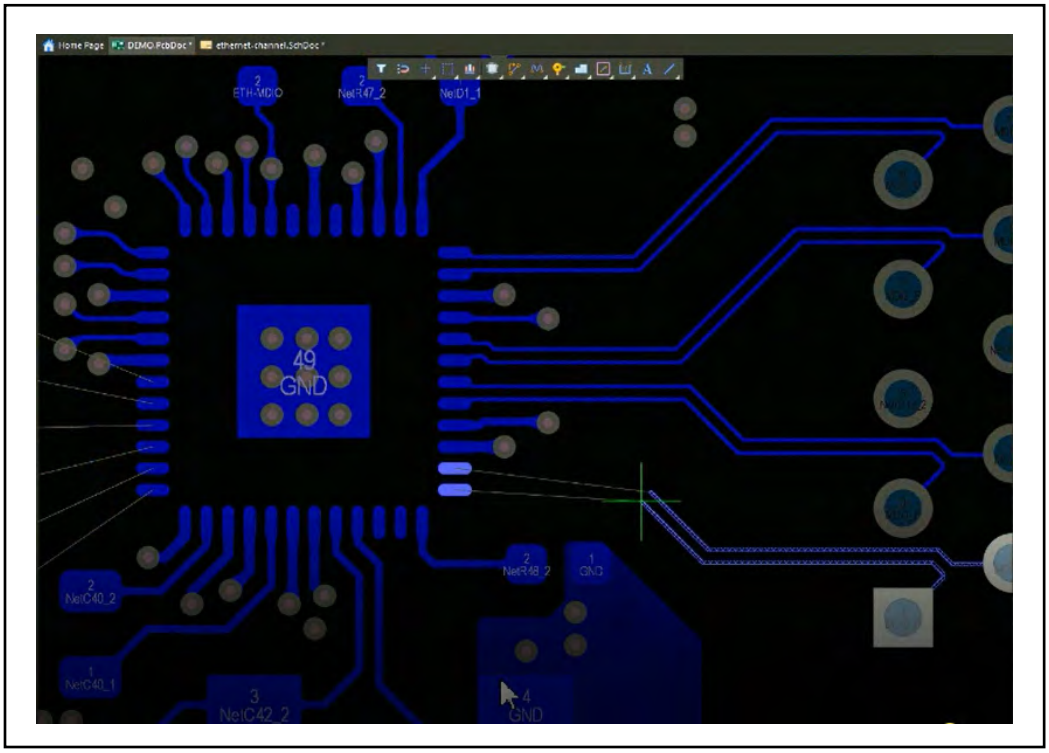
4.3 Routing

4.3.1 Differential pair routing

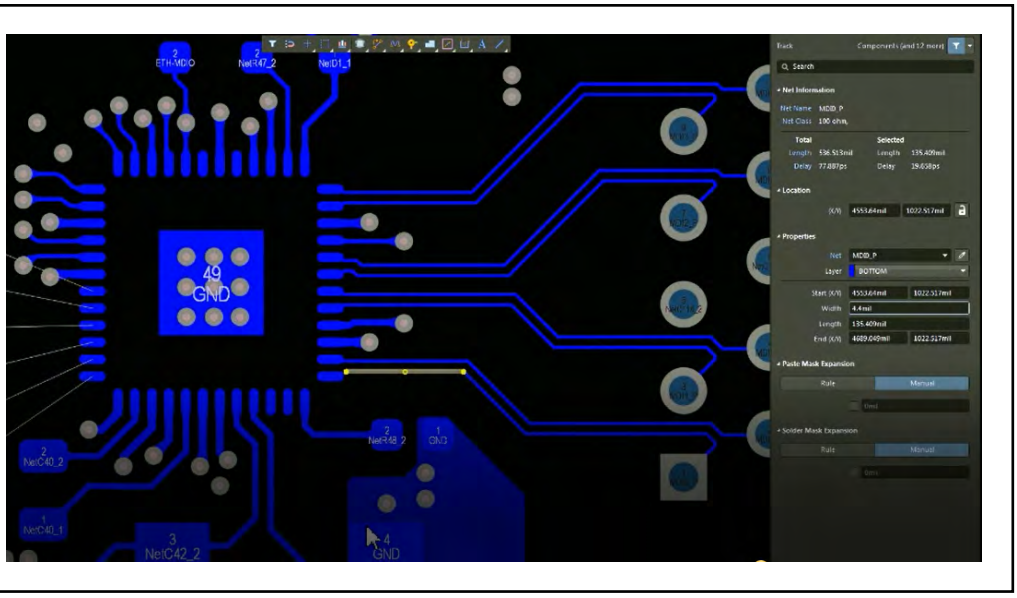
- For differential pair routing, go to **Interactive differential pair routing >> Route.**



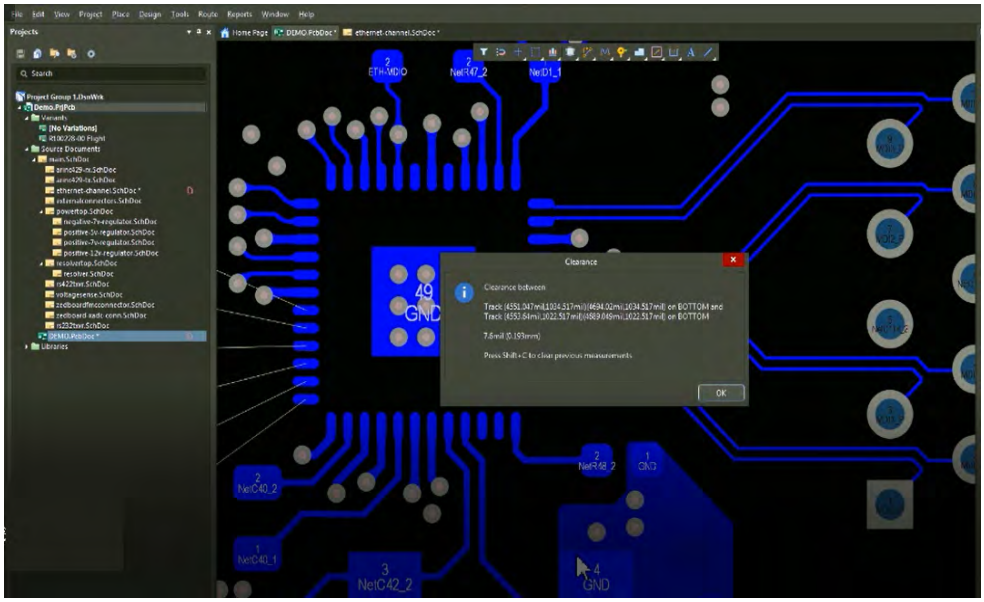
- Now, select the net and do the routing.



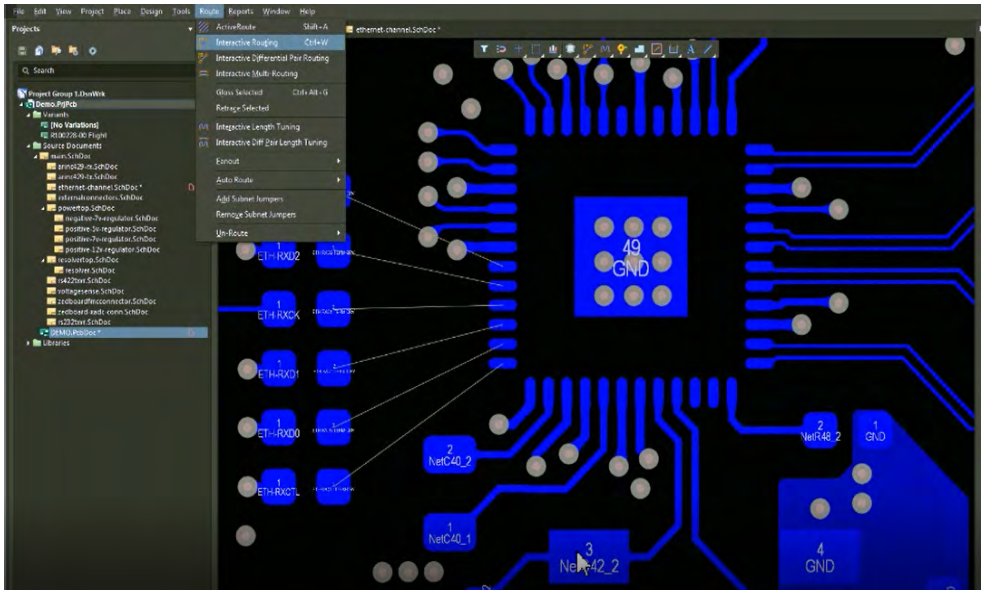
- After completing the routing step, check the values of these particular traces. Select any of the traces, go to properties, and check the values. Here, the trace width is 4.4mils, which is the same as given in the stack-up.



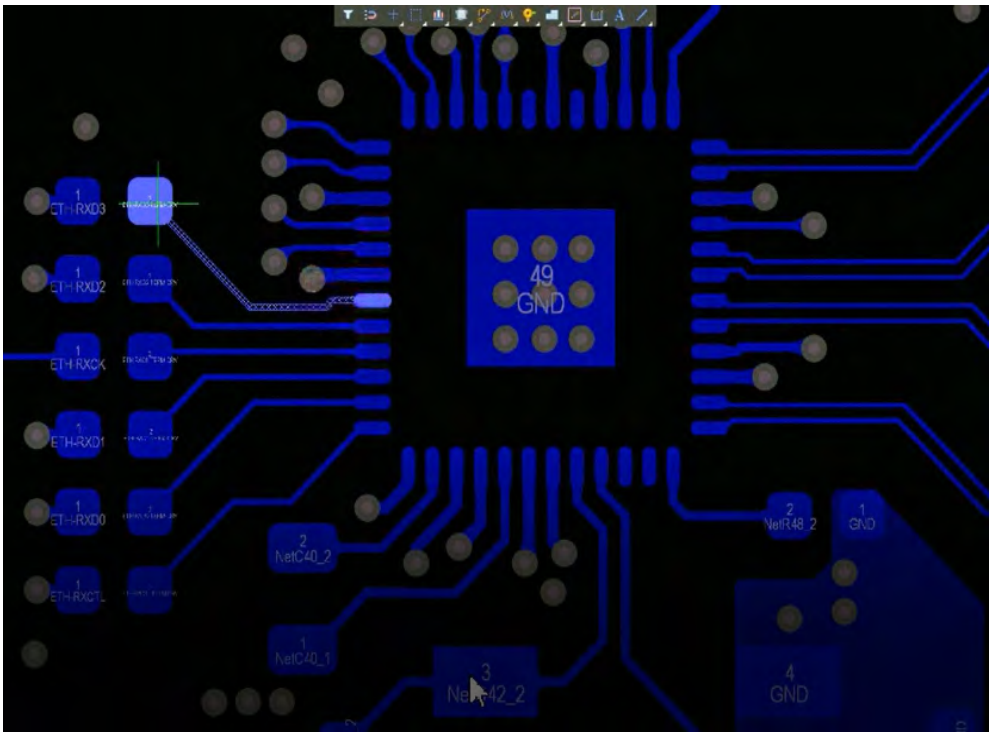
- Now go to report and measure primitives. Select the two traces that will give us the air gap between two traces (7.6mils), which is the same as the stack-up value.



4.3.2 Single-ended routing



- For single-ended routing, go to **Interactive routing >> Route** and repeat the above steps.



- Once the routing is done check the trace width.
- Select the trace under properties. You will see the trace width is 5.6mils that is the same as given in the stack-up.

Layers contain controlled impedance that is why we need to specify these impedances in the fab notes since there can be more than one value of impedance traces per layer. Separate aperture codes are defined for controlled impedance traces. We hope that our tutorial on controlled impedance routing using Altium Designer helps the designers to understand and follow the minute details while routing their PCB.

5

5. Sierra Circuits' capabilities

5.1 How Sierra checks for controlled impedance

Our planning department creates an impedance stack-up using hyperLynx field solver and a stack-up tool. We put in the values provided by the customer, and we adjust them according to suitability with manufacturing.

5.1.1 Controlled dielectric

If PCB designers choose to give us a controlled dielectric stack-up, we follow the controlled dielectric thicknesses provided. However, if impedance traces are not specified, thus manufacturing focus is completely upon building a board within +/- 10% tolerance of specified dielectric thickness from layer to layer.

5.1.2 Impedance control using TDR coupons

We control the impedance through dielectric thicknesses, trace width, and space. We perform a test to make sure we achieved the desired impedance using TDR coupons. First Articles are processed in order to evaluate any discrepancies before an entire order is committed. Adjustments are made depending upon results from the First Article to meet the customer's needs and manufacture boards within the specified tolerance.

A typical tolerance on final impedance is +/-10%. But Sierra is able to do +/-5% impedance tolerance.

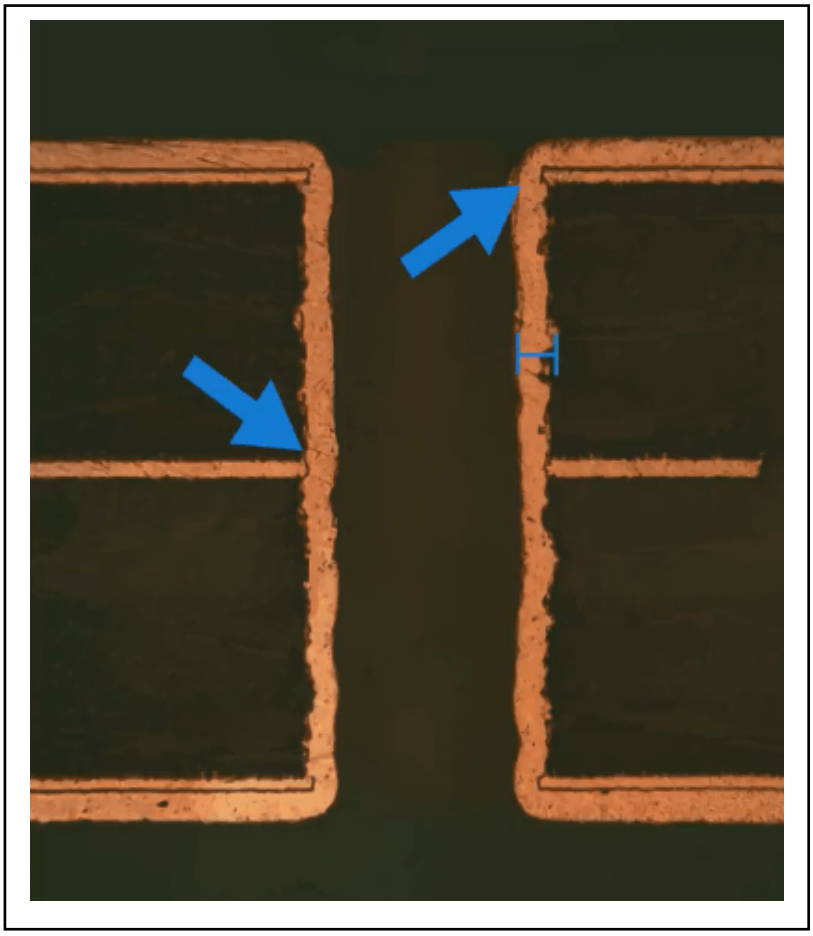
Equipment used by Sierra Circuits for impedance measurement:

1. Polar CITS – coupons only
2. Tektronix 8300 – boards as well as coupons

Suppose an impedance coupon is not functional or fails the impedance test. In that case, Sierra performs impedance testing on boards to verify if the product is within specifications or a remake would be required with necessary adjustments. However, it is critical to test impedance from boards due to the length of the traces on boards, which depends upon the board's size. The location of inner layer impedance traces on the finished product is very crucial as well.

5.1.3 Cross-section analysis

How do we ensure that you get what you are asking for? At Sierra, we perform cross-section analysis of the panel and measure the relevant thickness. This ensures a good connection to the inner layers and also the copper wrap is even throughout the hole. There are different requirements for IPC class 3 boards including CAF and etch-back.

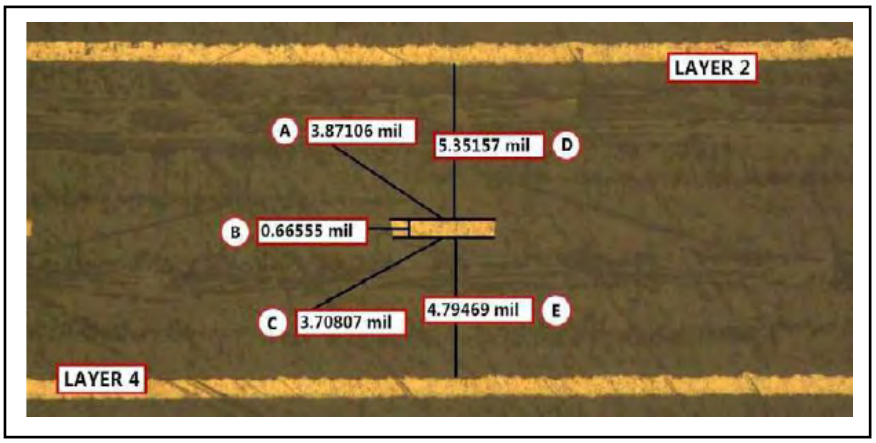


Upon failure, a cross-section is taken from the impedance coupon to further evaluate which factors are affecting the calculated impedance in relation to the recorded impedance. The cross-section technician measures dielectric thicknesses depending upon trace location, either inner layer or outer layer. Additionally, trace width is measured from the bottom as well as top of the affected impedance trace along with copper thickness or trace height.

In case of a differential pair, spacing between the two traces is also measured to understand if the projected impedance is in alignment with the recorded impedance or not.

The image below displays cross-section evaluation details on a single-ended impedance trace:

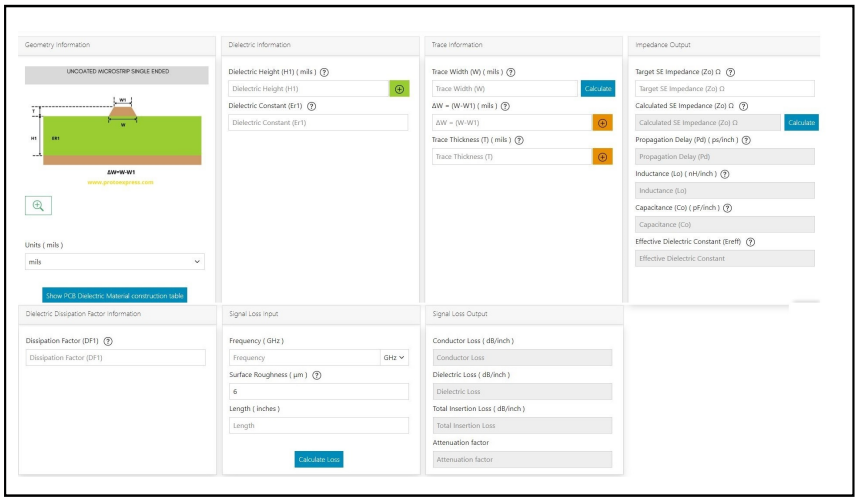
A – Trace width from top
B – Copper thickness or trace height
C – Trace width from bottom
D – Dielectric thickness between Layer 2 and Layer 3 (trace)
E – Dielectric thickness between Layer 3 (trace) and Layer 4



To determine the acceptability of the boards, we at Sierra Circuits use test coupons to make sure there are no variations in trace width, trace thickness, and so on. We manufacture the test coupons on the same panel and under the very same specifications than the actual boards – which are too difficult to test because of the controlled impedance traces that are hard to access and not often have any trace work or pads.

5.2 Sierra Circuit's Impedance Calculator

I



Our Impedance Calculator employs a 2D numerical solution of Maxwell's equations for PCB transmission lines. It provides accurate and suitable impedance values for circuit board manufacture. This calculator also estimates trace parameters such as capacitance, inductance, propagation delay per unit length, and the effective dielectric constant of the structure.

The tool features various microstrip and stripline structures for single-ended and differential models. Choose the right impedance calculator mode based on the geometry of the signal layer and the relevant reference plane(s).

Here, we'll have a look at the functionality of the coated microstrip single-ended impedance calculator.

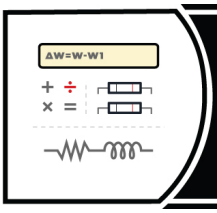
To calculate the single-ended impedance for a specific trace width, you will have to input the dielectric height, dielectric constants, trace width, delta w(ΔW), trace thickness, and coating heights.
Note: You can select the unit (mils/inches/mm/um/cm) of these parameters using the dropdown at the bottom left. Also, if you require any assistance with dielectric constant click on Show Material Dielectric Constant Guide. This shows the dielectric constant of various commonly used materials.
After providing all the necessary data, hit calculate besides the calculated SE impedance field.

The calculator now displays the values of the following parameters:

Calculated single-ended coated and uncoated impedance

- Propagation delay
- Inductance
- Capacitance
- Effective dielectric constant

If you would like to calculate the trace-width for a target impedance, you'll have to key in dielectric height, dielectric constants, ΔW, trace thickness, coating heights, and target impedance. Now, hit Calculate besides trace-width field to view the optimum trace-width for the given impedance.



Impedance Calculator

Try Now

6

6. About Sierra Circuits

6.1 About us

Sierra Circuits has been faithfully serving PCB designers and engineers since 1986, and has worked with over 20,000 customers since then. We specialize in PCB manufacturing and assembly and High-Density Interconnect technology. We handle all aspects of PCB production. Using Sierra, you can receive your fully-assembled boards in three days.

We provide our customers with unprecedented quality, reliability, and a single point of support. No more miscommunication between multiple vendors and no more delays. We are ISO-9001:2008, ISO 13485:2016 and MilSpec MIL-P-55110 certified.

6.2 Talk to our experts

Sierra Circuits helps PCB designers plan it right!

At Sierra Circuits, our engineering staff has been trained on controlled impedance and can analyze the design from a holistic point of view.

Our engineering support and our stack-up team provide valuable suggestions with their knowledge of controlled impedance for high-speed designs, analog/digital, high density PCB manufacturing design rules and design for assembly rules. Upload your data and receive a free consultation and review of your design. Services include system level design, schematic capture, PCB layout, and PCB/PCBA DFM.

SIERRA CIRCUITS

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